VIVEKANANDA COLLEGE
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NAAC ACCREDITED 'A' GRADE

Topic: counter- part 2

Course Title: Digital Electronics and VHDL

Paper: ELT-A-CC-4-09-TH

Unit: Sequential Circuit

Semester: Fourth

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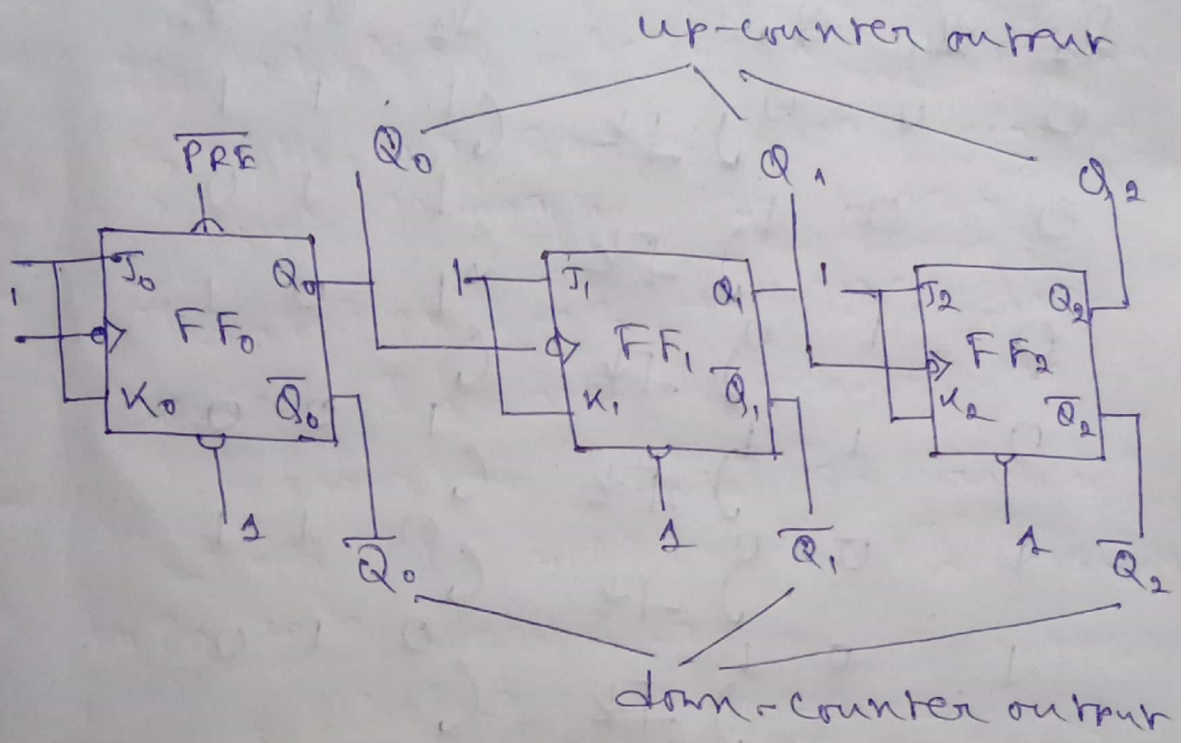
Name of the Department: Electronic Science

Asynchronous up/Down Counter

3 bit Binary ripple up-down counter :—



From this fig we can see that the Q-output gives us the up-count sequence. If a link is set-up Between Q-output of one flip-flop to the clock input of the next, we can see that the down count sequence is obtained from $\overline{Q}$ output.
If the connection is made Between $\overline{Q}$ to clock input. Now the two count sequences can be obtained from a single circuit.

The count sequence of 3-bit binary up/Down counter is →

Q_2	Q_1	Q_0	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

→ Conversion from up-counter to down counter.

i) The flip-flops are all negative edged triggered.

ii) The Q- output of a flip-flop connect the clock input of the next one.

iii) The counter output is taken from the Q-output

If the change any one of three feature the circuit will be count down-counter.