VIVEKANANDA COLLEGE
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NAAC ACCREDITED 'A' GRADE

Topic: VHDL_1

Course Title: Digital Electronics and VHDL

Paper: CC-9

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VHDL :-

- Is a hardware language.
- Full form of VHDL is VHSIC HDL or very high speed integrated circuit Hardware Description language.
- It is used for Digital IC and not for analog IC.
- VHDL uses gate level design abstraction

History :-

1. Department of Defence - 1980-87
2. 1987 ⇒ got IEEE.
3. 1993 = revised edition (not synthesizable in this period).
4. 1996 = revised further (It is synthesized language and simulation tools were added).
5. ~~VHDL is~~

VHDL vs C

- VHDL is concurrent language while 'C' is Sequential.
- VHDL is synthesizable while 'C' is not.

Capability

- Case insensitive language.
- Vendor independent [Xilinx, Altera, Modelsim]
- It support Synthesis.
- It support simulation.

VHDL Capabilities

It support 9 value logic system :-

'0' = strong zero.
'1' = strong One.
'L' = ~~low~~ weak zero.
'H' = weak One.
'Z' = High Impedance or strong Translab.
'W' = low " or ~~low~~ weak ".

'U' = Uninitializ.
'X' = Foreign Unknown.
'-' = Don't Care

Program structure in VHDL :-

1. Library.
2. Entity.
3. Architecture

1.

```
Library ieee;
Use ieee.std_logic_1164.all;
```

- Using IEEE library. → use above package completly.
- Use std_logic_1164 package of the library.

2. (It is used to declare i/p o/p port.)

```
entity abcd is
port ( a: in std_logic;
       b: in std_logic;
       c: out std_logic);
end abcd;
```

abcd → name of entity.
a → variable
in → i/p
std_logic → datatype
; → termination
bit, billium, variable.

3. Architecture (we write logic of program).

```
architecture myabcd of abcd is
begin
output <= input1 and input2;
end myabcd;
```

myabcd → name of architecture

Types of Modeling Style:-

- Data flow modeling
- Behavioral modeling.
- Structural modeling.
- Hybrid modeling.

VHDL Operators:-

- Logical Operators.
- Relational "
- Shift "
- Adding "
- Multiplying "
- Miscellaneous ".

Logical operator:-

and, or, nand, nor, xor, xnor, not

Relational Operator:-

=, /=, <, <=, >, >=

Shift operators:-

SLL = Shift logical left.
SRL = " " right.
SLA = " arithmatic left.
SRA = " " right.
ROL = rotate left.
ROR = " right.

0011 SLL 1 = 0110
1100 SRL 2 = 0011
1100 SLA 1 = 1000 (See right most is '0', insert '0')
1100 SRA 2 = 1111 (See left most is '1', insert '1')
1010 ROL 1 = 0101
0011 ROR 1 = 1001 (1100 ROR-1 = 1100 ROL 1 = 1001)