VIVEKANANDA COLLEGE
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NAAC ACCREDITED 'A' GRADE

Topic: Combinational logic analysis and design _3

Course Title: Digital Electronics and VHDL

Paper: CC-9

Unit:

Semester: 4

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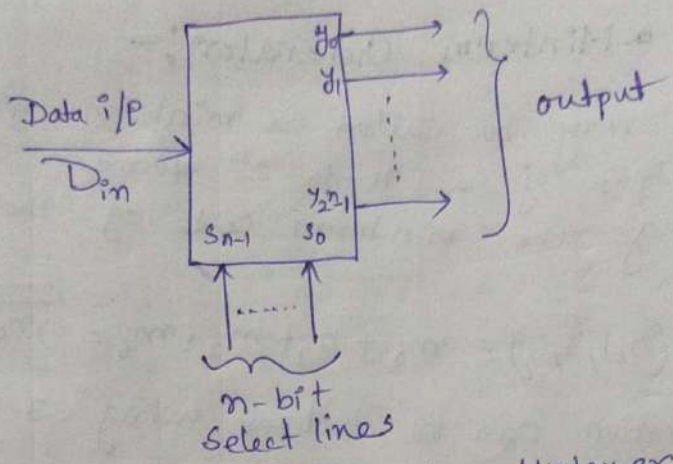
Name of the Department: Electronics

Demultiplexer: This is a logic circuit functionally reverse of a multiplexer. This circuit receives data on an input line and routes this received data on one of 2^n possible output lines. The output line through which the data will be routed is determined by the n- Bit Select code applied to the Select inputs.



Block diagram of demultiplexer.

If there are n=4 select lines, there should be $2^4=16$ outputs.

Design of 1-to-4 Demultiplexer:

Let us consider the following table of a demultiplexer which is having 4 active low outputs $\overline{Y_0}, \overline{Y_1}, \overline{Y_2}, \overline{Y_3}$. Therefore, two Select lines (B and A) are required to route the received data (Din) through one of the four outputs.

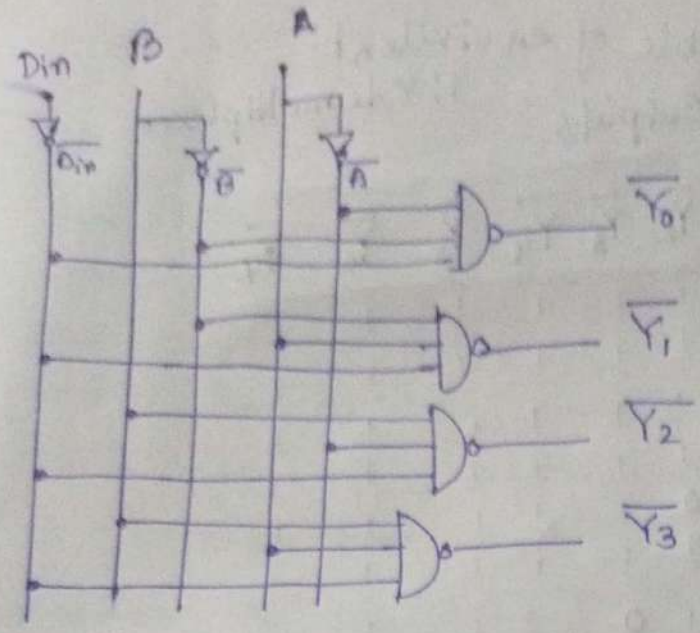
Data i/p	Select lines		output			
Din	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$
0	0	0	0	1	1	1
1	0	0	1	1	1	1
0	0	1	1	0	1	1
1	0	1	1	1	1	1
0	1	0	1	1	0	1
1	1	0	1	1	1	1
0	1	1	1	1	1	0
1	1	1	1	1	1	1

$$\overline{Y_0} = \overline{(\overline{B}.\overline{A})\,\overline{Din}}$$

$$\overline{Y_1} = \overline{(\overline{B}.A)\,\overline{Din}}$$

$$\overline{Y_2} = \overline{(B.\overline{A})\,\overline{Din}}$$

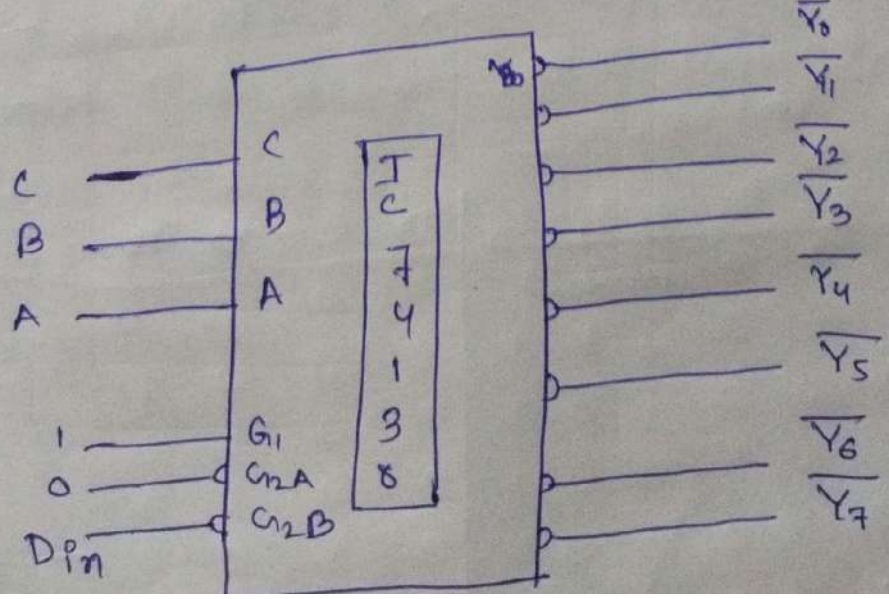
$$\overline{Y_3} = \overline{(B.A)\,\overline{Din}}$$



1 to 4 demultiplexer.

IC 74138 As 1-to-8 Demultiplexer :-

Ic 74138 (3-to-8 decoder) can be used as an 1-to-8 demultiplexer if we consider enable inputs as data inputs. Let us consider $\overline{G_{2B}}$ enable input as the data input (Din). The data Din can be routed through any one of the eight output. The selection of the output through which the data input will pass through is selected by the select lines CBA.



Function table of equivalent 1:8 demultiplexer

Inputs						Outputs							
Enable i/p		Data i/p	Select i/p										
G_1	$\overline{G_{2A}}$	D_{in}	C	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	1	0	0	0	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	1	0	1	0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1

Encoders and Priority encoders:

An encoder performs the opposite function of a decoder. Thus, an encoder is a logic circuit whose each input is a piece of information and the outputs are the uniquely coded representation of these inputs. The number of bits required for such encoding depends on the number of elements of inputs. For n elements of information the number of to be uniquely encoded, the output code of width m must satisfy the relation $2^m \geq n$. For eg→ to encode 10 decimal digits distinctly we need a group 4 binary bits. The drawback of this simple encoder is that this encoder circuit cannot encode properly if more than one input active simultaneously. To prevent this odd situation a new type of encoder circuit is designed which is called "Priority encoders".

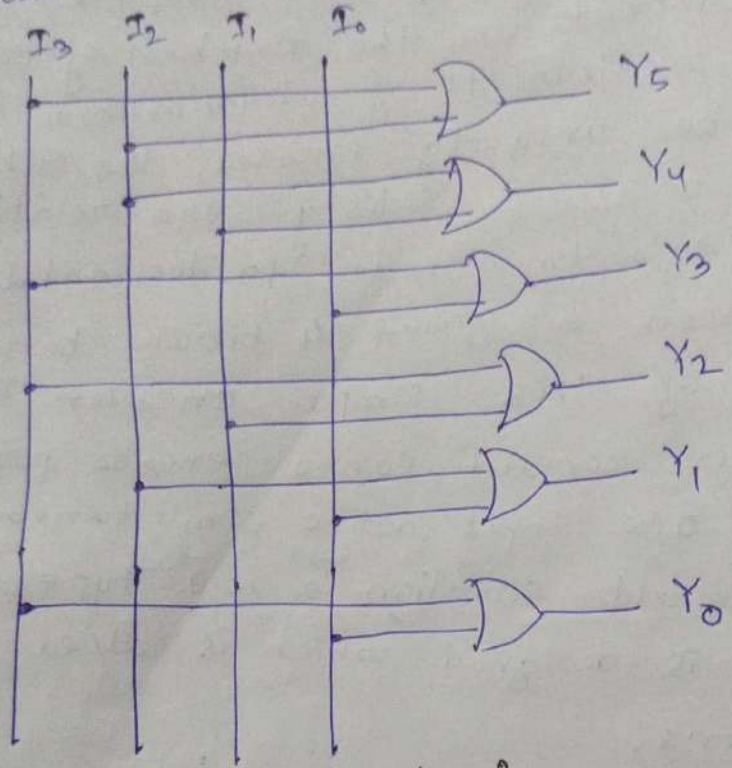
Design of ordinary encoder circuit:

Design an encoder circuit which has 4 active high inputs I_3, I_2, I_1 and I_0. This circuit needs to produce 6-bit distinct code for each input as shown in table below. The restriction regarding the inputs is that only one input may be active at a time.

Input				output					
I_3	I_2	I_1	I_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
1	0	0	0	1	0	1	1	0	1
0	1	0	0	1	1	0	0	1	0
0	0	1	0	0	1	0	1	0	0
0	0	0	1	0	0	1	0	1	1

So, $Y_5 = I_3 + I_2$, $Y_4 = I_2 + I_1$,
$Y_3 = I_3 + I_0$, $Y_2 = I_3 + I_1$,
$Y_1 = I_2 + I_0$, $Y_0 = I_3 + I_0$

from the expressions,



Decimal to-BCD Encoder:

In this encoder 10 inputs (I_0 to I_9) each input represent a decimal digit. The o/p of this encoder has 4 parallel o/ps. (D, C, B, A). Each 4 bit output correspond to BCD code of the input line.

Input										Output			
I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D	C	B	A
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

There force from the table :—

$$D = I_8 + I_9$$

$$C = I_4 + I_5 + I_6 + I_7$$

$$B = I_2 + I_3 + I_6 + I_7$$

$$A = I_1 + I_3 + I_5 + I_7 + I_9$$

and the following circuit is ⟶