VIVEKANANDA COLLEGE
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NAAC ACCREDITED 'A' GRADE

Topic: Combinational logic analysis and design _2

Course Title: Digital Electronics and VHDL

Paper: CC-9

Unit:

Semester: 4

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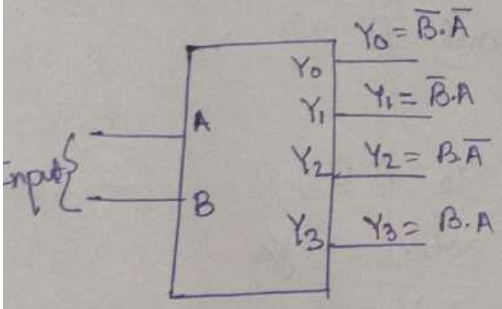
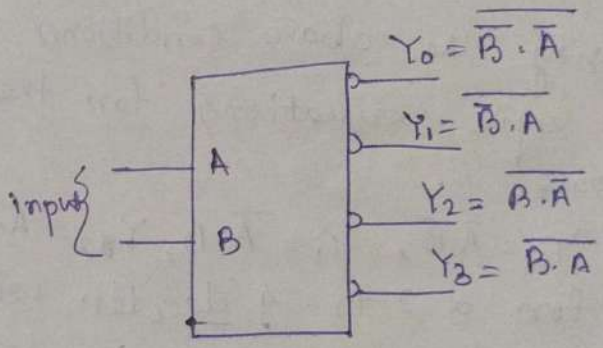
Name of the Department: Electronics

Decoder:-

A decoder is a combinational circuit with n-bit input and m number of mutually exclusive outputs. The mutually exclusive output means that the decoder circuit makes only one output (active high or active low) among the m possible outputs and this output is unique and depends on the input code applied to the n-bit input. using these n-bits we can have maximum 2^n codes, so the maximum number of mutually exclusive output may be $m = 2^n$. If there are two input (i.e $n=2$), we have $2^2 = 4$ no of codes and therefore the no of mutually exclusive outputs is $m=4$. So when $n=2$ and $m=4$ the decoder is known as 2-to-4 decoder.



2 to 4 decoder with active high outputs



2 to 4 decoder with active low outputs.

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Input		outputs			
B	A	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

⇓

Input		outputs			
B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Design of A 2-to 4 Decoder :-

i) if the inputs A B = 0 0 = 2-bit minterm code of m_0 at the input then only $Y_0 = 1$ for active high o/p
$\overline{Y_0} = 0$ for active low o/p

ii) if AB = 01 = 2-bit minterm code of m_1 at the input then only $Y_1 = 1$ for active high o/p
$\overline{Y_1} = 0$ for active low o/p

iii) if AB = 10 = 2-bit minterm code of m_2 at the input then only $Y_2 = 1$ for active high o/p
$\overline{Y_2} = 0$ for active low o/p

iv) if AB = 11 = 2-bit minterm code of m_3 at the input then only $Y_3 = 1$ for active high o/p
$\overline{Y_3} = 0$ for active low o/p

Using the above conditions we may write the logic equations for the outputs as follows:

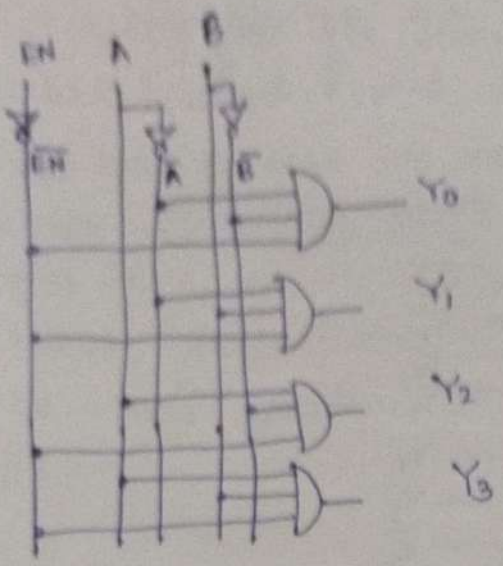
i) $Y_0 = \bar{A}\bar{B}$, $Y_1 = \bar{A} \cdot B$, $Y_2 = A \cdot \bar{B}$, $Y_3 = A \cdot B$; for a 2-to-4 decoder with active-high outputs.

ii) $\overline{Y_0} = \overline{\bar{A} \cdot \bar{B}}$, $\overline{Y_1} = \overline{\bar{A} \cdot B}$, $\overline{Y_2} = \overline{A \cdot \bar{B}}$, $\overline{Y_3} = \overline{A \cdot B}$; for a 2-to-4 decoder with active-low outputs.

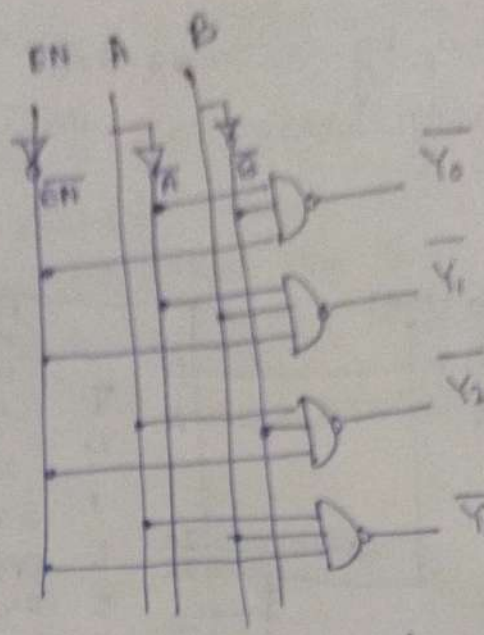
If we include enable,

A) $Y_0 = \bar{A}\bar{B} \cdot \overline{EN}$, $Y_1 = \bar{A} \cdot B\,\overline{EN}$, $Y_2 = A \cdot \bar{B}\ \overline{EN}$
$Y_3 = A \cdot B\,\overline{EN}$ for active high outputs.

B) $\overline{Y_0} = \overline{\bar{A} \cdot \bar{B}\ \overline{EN}}$ $\overline{Y_1} = \overline{\bar{A} \cdot B\ \overline{EN}}$ $\overline{Y_2} = \overline{A \cdot \bar{B}\ \overline{EN}}$
$\overline{Y_3} = \overline{A \cdot B \cdot \overline{EN}}$ for active low outputs.



2-to-4 decoder with high o/p

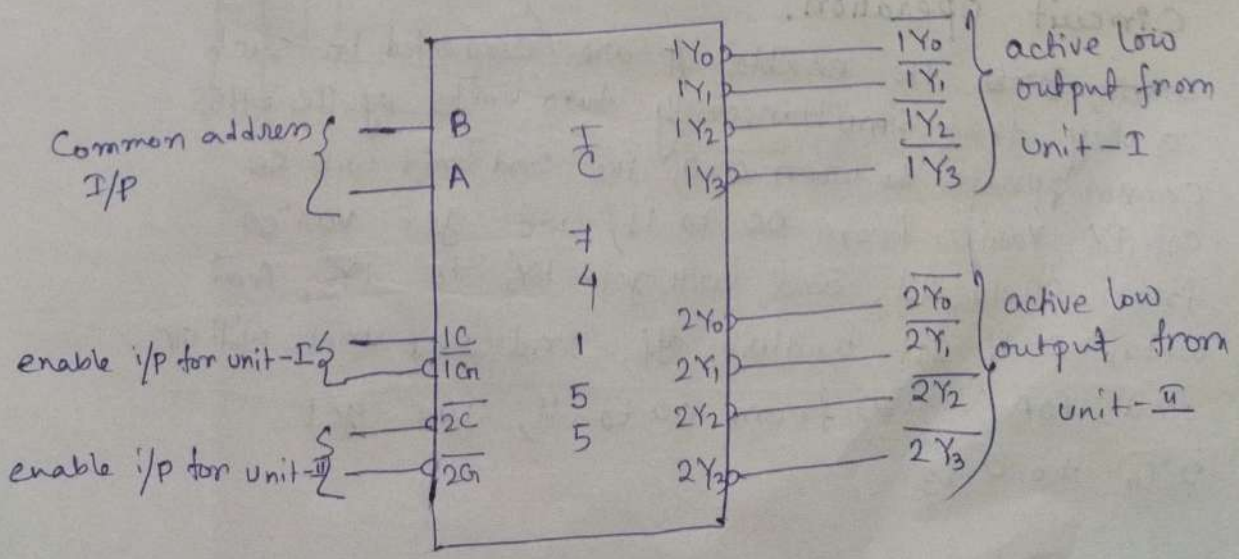


2 to 4 decoder with low o/p

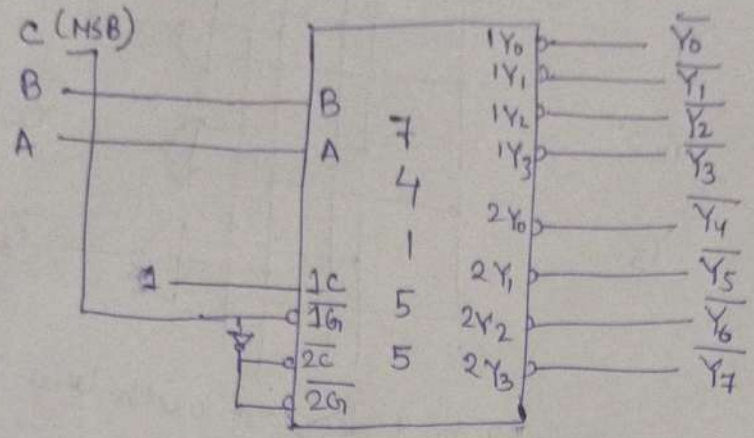
Cascading of Decoders:-

- Cascading two 2-to-4 decoders to obtain a 3-to-8 decoder:

For this purpose we would use IC 74L55 which is a popular 2-to-4 decoder. This decoder IC chip has two units. Unit-I has two enable inputs- one active high and one active low. But the unit-II has two active low enable inputs. It has two common address lines.



Now, by cascading these two units we may easily have an equivalent 3-to-8 decoder.



Now the function table:→

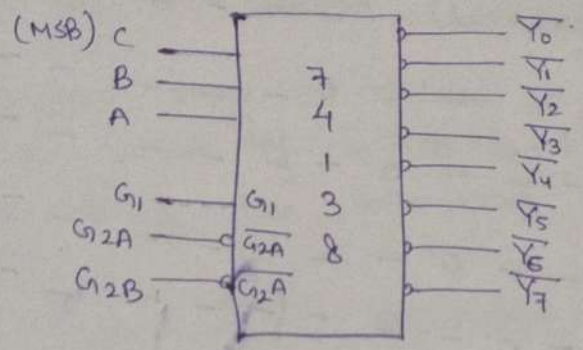
Inputs				Outputs							
Enable I/P	Address line			$\overline{1Y_0}$	$\overline{1Y_1}$	$\overline{1Y_2}$	$\overline{1Y_3}$	$\overline{2Y_0}$	$\overline{2Y_1}$	$\overline{2Y_2}$	$\overline{2Y_3}$
1C	C	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

Circuit operation:

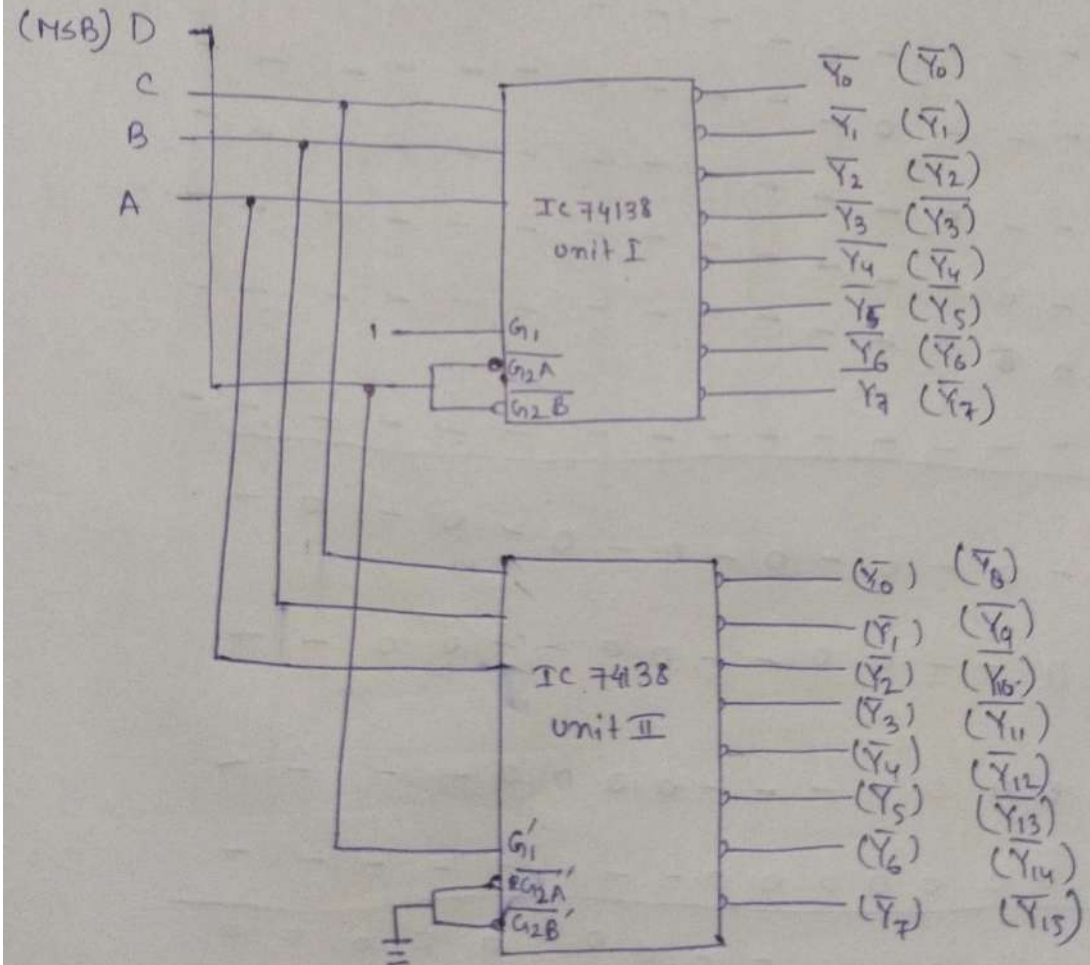
The enable i/p are connected in such a way that simultaneously two units of IC 74155 cannot operate. When C=0, the 2nd unit will be off, BA varies from 00 to 11, we get varies from 00 to 11, and will get $\overline{1Y_0}$ to $\overline{1Y_3}$. And when C=1, 1st unit will off and 2nd unit will on and BA varies from 00 to 11, we get $\overline{2Y_0}$ to $\overline{2Y_3}$.

Cascading of two 3 to 8 decoders to obtain a 4 to 16 decoder :-

for this purpose we would use a popular 3-to-8 decoder IC chip 74138. It contain three address inputs (C, B, A) and 8 active low o/Ps. There are 3 enables i/Ps — one active high (G_1) enable input and two active low (G_{2A} and G_{2B}) enable i/Ps.



Now by using IC 74138 we can make 4-to-16 decoder



Block diagram

Function Table

Enable I/P			Address I/P				output											
G_1	G_{2A}'	G_{2B}'	D	C	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$	$\overline{Y_8}$	$\overline{Y_9}$	$\overline{Y_{10}}$	$\overline{Y_{11}}$	$\overline{Y_{12}}$	$\overline{Y_{13}}$	$\overline{Y_{14}}$	$\overline{Y_{15}}$
1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Circuit operation :-

When D=0, unit I will be on and unit-II will be off. for the eight combination of CBA starting from 000 to 111, we get active low o/ps from $\overline{Y_0}$ to $\overline{Y_7}$ from unit I.

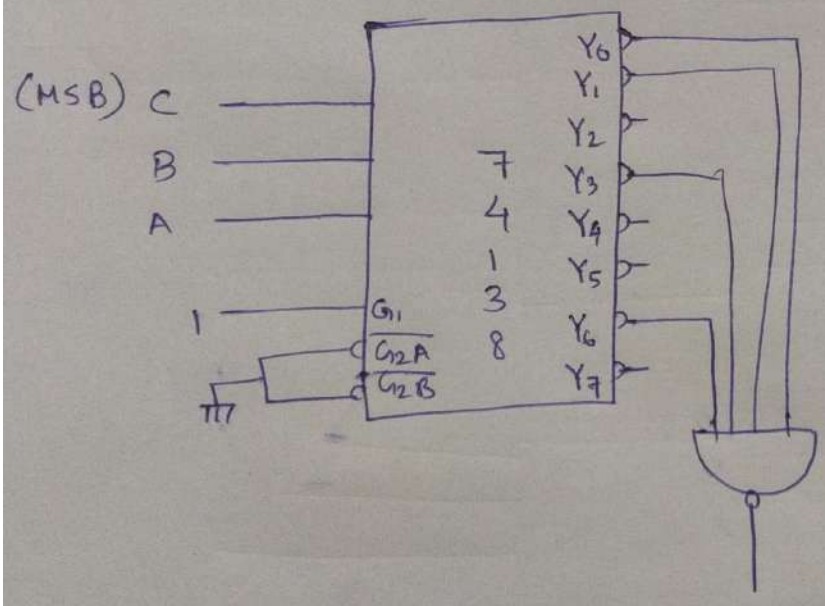
When D=1, unit I will be off and unit II will be on. Then, for the eight input combinations of CBA, we get active low o/ps through the pin $\overline{Y_8}$ to $\overline{Y_{15}}$ from unit -II.

Decoder as a Minterm Generator :-

A decoder may be called a minterm generator because the output of a n-to-2^n decoder can be expressed using the minterm code of the n input variables.

$$F = \Sigma m(0,1,3,6) = m_0 + m_1 + m_3 + m_6 = \overline{m_0 \cdot m_1 \cdot m_3 \cdot m_6}$$

the above function can be realized using 3-to-8 decoder,



$F = \Sigma m(0,1,3,6)$