VIVEKANANDA COLLEGE
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NAAC ACCREDITED 'A' GRADE

Topic: MOSFET introduction and enhancement mode

Course Title: Electronics device and circuit

Paper: CMS-A-CC-2-4-TH

Unit: Unipolar junction transistor

Semester: second

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Name of the Department: Electronic Science

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MOSFET

Metal- Oxide- Semiconductor-FET

It is also referred as IGFET (insulated-Gate-FET), MISFET (Metal-Insulator-FET)

The MOSFET transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in electronic dev

The MOSFET is a four termin device with Source (S), Gate (G), drain (D) and Body. The body of the MOSFET is connected to th source terminal so making it a three terminal device.

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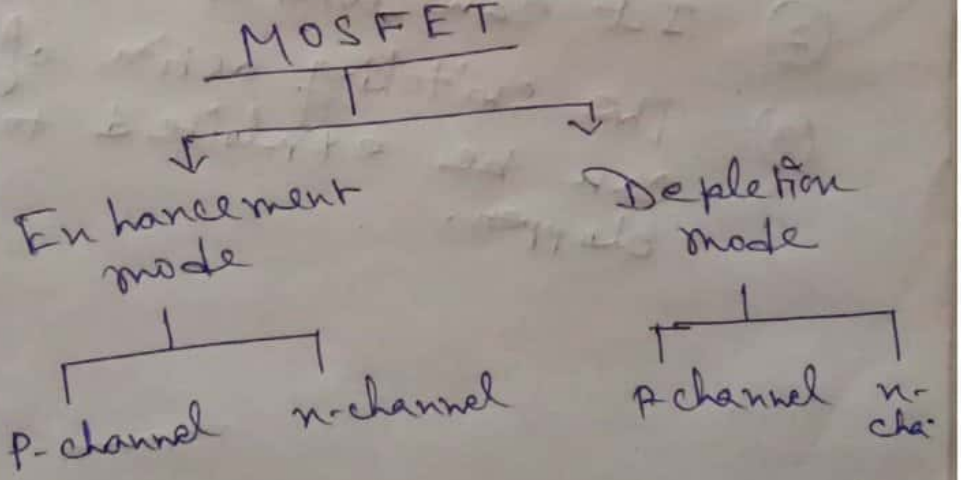
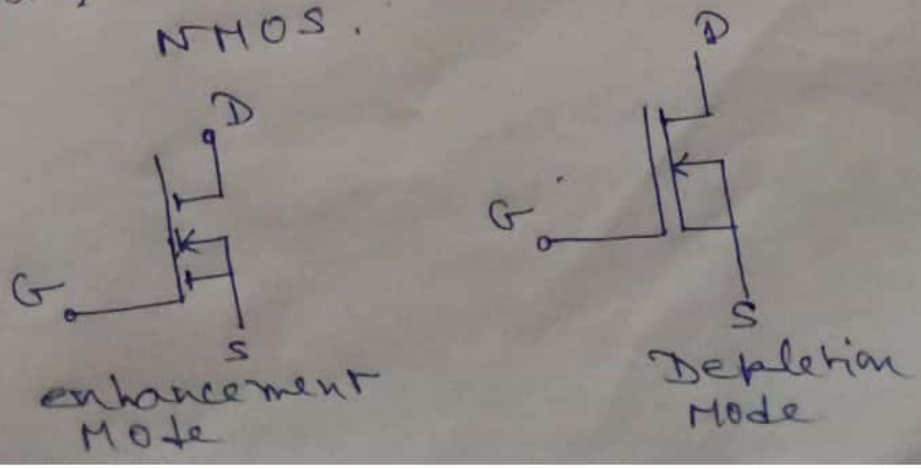
Construction of MOSFET

In case of MOS, an oxide layer is deposited on the substrate to which the gate terminal is connected. This oxide layer acts as insulator a lightly doped substrate is diffused with a heavily doped region. Depending upon the substrate, they are called as P-type and N-type MOSFETs

Classification :-



→ N channel MOSFET is called NMOS.



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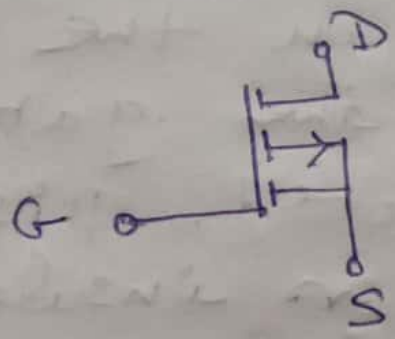
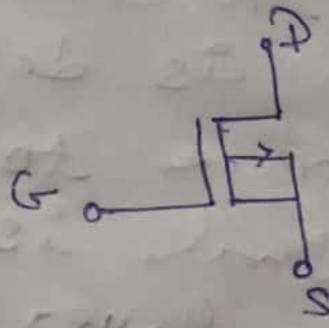
→ P-channel MOSFETs are called P-MOS.



Enhancement Mode



Depletion Mode

Application of MOSFET →

1. MOSFET can act as a switching circuit
2. It can use as amplifier
3. The switching action of MOSFET can be exploited to design chopper.

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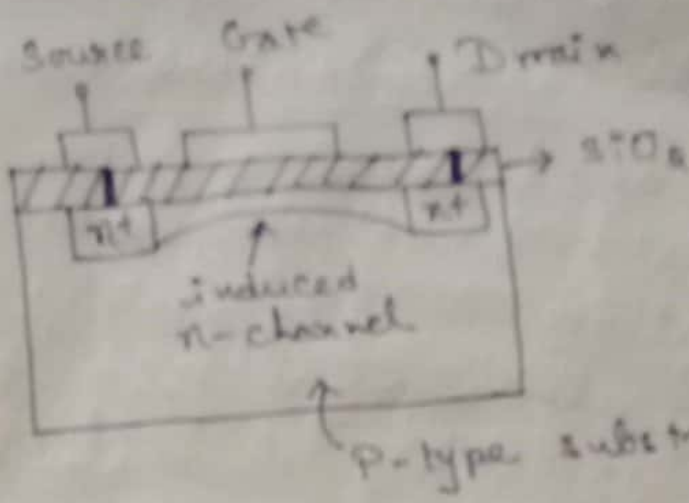
n - channel enhancement MOSFET



A schematic diagram of n-channel enhancement MOSFET.

Description:- There is a lightly but uniformly doped p-type substrate at the top surface of the substrate two n^+ region (heavily doped) are formed. A thin layer of SiO_2 is diposited on the top surface of the substrate. There are two ohmic contacts which connect the two n^+ region with source and drain terminal of the device. At the middle of SiO_2 layer a metal electrod is formed called the gate of the device.

Operation:- If there is no voltage at the gate terminal, there will be no induced channel between n^+ region so no current flows through the device.

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where positive voltage is applied to the Gate terminal with respect to source due to capacitive action. The negative carriers are accumulated just below the SiO_2 layer. This results an n-channel between the two n^+ regions. By varying the Gate voltage one can change the conductivity of n-channel and hence the drain current.

Why the input impedance of MOSFET is very high?

In this device between gate and p-type substrate a thin layer of SiO_2 is there, so practically, there is no flow of current (small likage current) between Gate and substrate, therefore input impedance is so high (10^4-10^9 MΩ)

Threshold voltage of enhancement MOSFET ⟶

The threshold voltage is defined as Gate-Source voltage at which the drain current per unit width reaches some defined small value (1mA)

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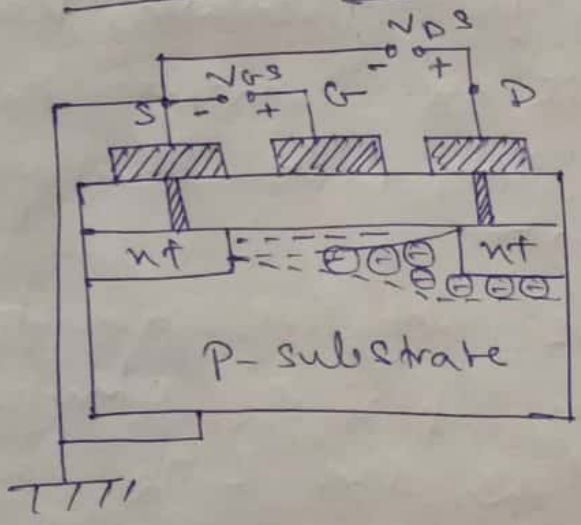
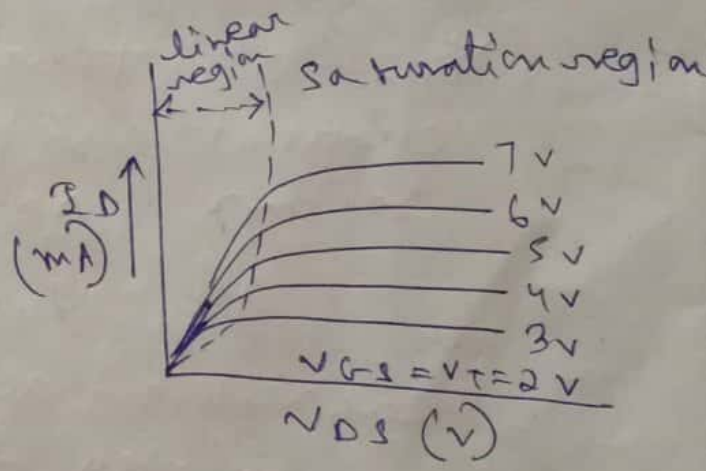
Drain characteristics of N MOSFET (enhancement type)





The variation of the drain current I_D with V_{DS} at a constant V_{GS} is defined as drain characteristic of MOSFET

when $V_{GS} < V_T$, there is no channel induced between two n+ regions, I_D is '0', when $V_{GS} > V_T$, the channel is induced and I_D increases linearly for a small increase in V_{DS}. MOSFET act as a resistor in this region which is called Linear region.

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For a particular value of $V_{GS} > V_T$, when V_{DS} increases the depletion region is formed between n^+ regions and p-type substrate at the drain end. when the electrons flow through this depletion region, they experienced high resistance. current becomes almost saturate and the channel is pinch-off by the depletion region.

If V_{DS} is increased to a fairly high value avalanch breakdown may occur causing a large flow of current which may damage the device

for linear region →

$$I_D = 2K (V_{GS} - V_T) V_{DS}$$

$$I_D \propto V_{DS}$$

at pinch off $[V_{GS} - V_T = V_{DS}]$

$$\therefore I_D = 2K V_{DS}^2$$

$$I_D \propto V_{DS}^2$$

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