VIVEKANANDA COLLEGE
THAKURPUKUR
KOLKATA-700063

NAAC ACCREDITED 'A' GRADE

Topic: Combinational logic analysis and design

Course Title: Digital Electronics and VHDL

Paper: CC-9

Unit:

Semester: 4

Name of the Teacher: Sanchari Guha

Name of the Department: Electronics

1 bit magnitude Comparator :-

Magnitude comparator compares the magnitude of two numbers expressed in binary.

The truth table of 1 bit magnitude comparator is given below :→

A magnitude comparator circuit gives three possible outputs — $(A=B)_0$, $(A>B)_0$, $(A<B)_0$.

Input		output		
A	B	$(A>B)_0$	$(A=B)_0$	$(A<B)_0$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

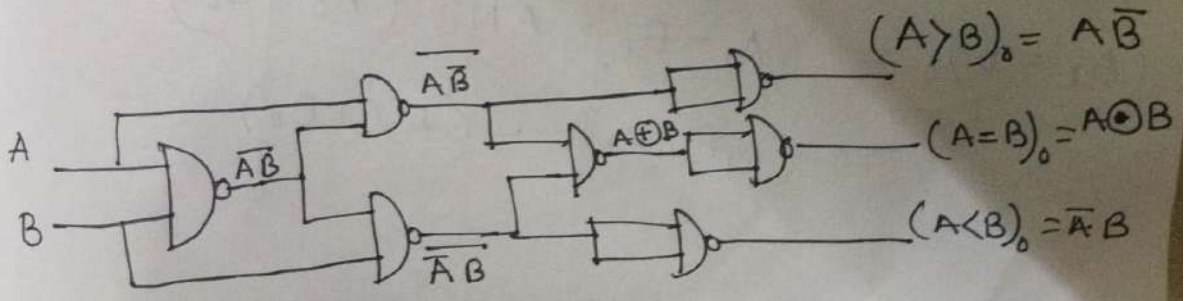
The following logic expressions :—

$(A>B)_0 = A \cdot \overline{B}$

$(A<B)_0 = \overline{A}\,B$

$(A=B)_0 = \overline{A} \cdot \overline{B} + A \cdot B = A \odot B$.

There fore the logic circuit →



2 bit magnitude Comparator :-

The 2 bit magnitude comparator compares two variables, say A and B. Each of the variables contains 2 bits, individual. Therefore $A = A_1 A_0$ and $B = B_1 B_0$.

(i) when the magnitude of the variable A is equal to that of variable B, $(A=B)_0$ becomes HIGH.

(ii) when the magnitude of variable A is greater that that of variable B, $(A>B)_0$ output becomes HIGH.

(iii) when the magnitude of the variable A is smaller than that of the variable B, $(A<B)_0$ become high.

So the output will be,

$$(A>B)_0 = (A_1 > B_1) \text{ OR } (A_1 = B_1) \text{ AND } (A_0 > B_0)$$

$$= A_1 \overline{B}_1 + (A_1 \odot B_1)(A_0 \overline{B}_0)$$

$$(A<B)_0 = (A_1 < B_1) \text{ OR } (A_1 = B_1) \text{ AND } (A_0 < B_0)$$

$$= \overline{A}_1 B_1 + (A_1 \odot B_1)(\overline{A}_0 B_0)$$

$$(A=B)_0 = (A_1 = B_1) \text{ AND } (A_0 = B_0)$$

$$= (A_1 \odot B_1) \cdot (A_0 \odot B_0)$$

4 bit magnitude comparator :-

(Variable)

$A = A_3\ A_2\ A_1\ A_0$ (A_3 = MSB, A_0 = LSB)

$B = B_3\ B_2\ B_1\ B_0$ (B_3 = MSB, B_0 = LSB)

So there can be three cases.

Case 1 $\Rightarrow \underline{(A=B)_0} \Rightarrow (A_3 = B_3)$ and $(A_2 = B_2)$ AND $(A_1 = B_1)$ AND $(A_0 = B_0)$

$\Rightarrow (A_3 \odot B_3)\ (A_2 \odot B_2)\ (A_1 \odot B_1)\ (A_0 \odot B_0)$

Case 2 $\Rightarrow \underline{(A > B)_0} \Rightarrow (A_3 > B_3)$ OR $(A_3 = B_3)$ AND $(A_2 > B_2)$ OR $(A_3 = B_3)$ AND $(A_2 = B_2)$ AND $(A_1 > B_1)$ OR $(A_3 = B_3)$ AND $(A_2 = B_2)$ AND $(A_1 = B_1)$ AND $(A_0 > B_0)$

$\Rightarrow A_3 \bar{B}_3 + (A_3 \odot B_3)(A_2 \bar{B}_2) + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \bar{B}_1) + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \bar{B}_0)$

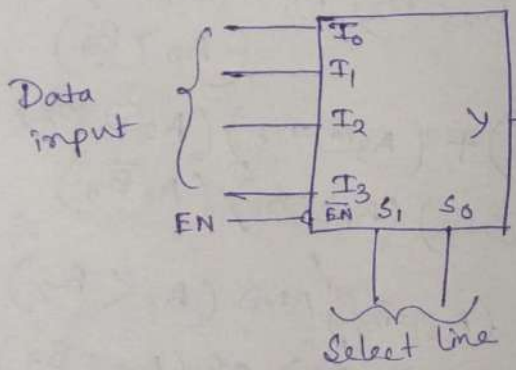
Case 3 $\Rightarrow \underline{(A < B)_0} \Rightarrow (A_3 < B_3)$ OR $(A_3 = B_3)$ AND $(A_2 < B_2)$ OR $(A_3 = B_3)$ AND $(A_2 = B_2)$ AND $(A_1 < B_1)$ OR $(A_3 = B_3)$ AND $(A_2 = B_2)$ AND $(A_1 = B_1)$ AND $(A_0 < B_0)$

$= \bar{A}_3 B_3 + (A_3 \odot B_3)(\bar{A}_2 B_2) + (A_3 \odot B_3)(A_2 \odot B_2)(\bar{A}_1 B_1) + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(\bar{A}_0 B_0)$

MULTIPLEXER :-

Multiplexing means transmitting a large number of information units over a small number of channels or lines. The multiplexer ~~is a~~ circuit in general may have M data inputs and are o/p line. The relationship between this M and N is $M = 2^N$. where M = data input and N = select lines. The MUX with M input and 1 output is mentioned as ~~M and~~ (M×1) or M-to-1 MUX or as M: 1 MUX.

Design of A 4:1 MUX :



I_0 to I_3 these four lines are inputs. Y is ~~at~~ only one input. S_1, S_0 are the ~~to~~ Select line.

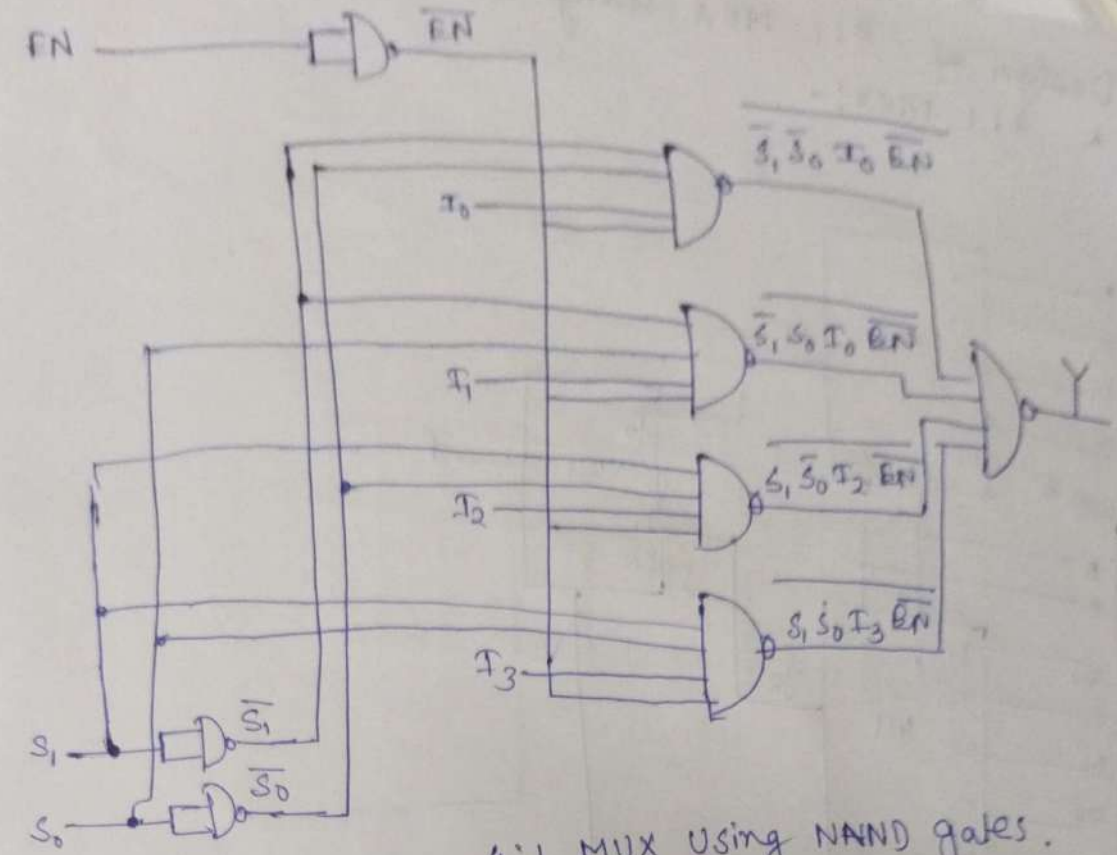
Function table of a 4:1 MUX :-

Enable	Select Inputs		Selected input	Output
EN	S_1	S_0		Y
0	0	0	I_0	I_0
0	0	1	I_1	I_1
0	1	0	I_2	I_2
0	1	1	I_3	I_3
1	X	X	None	0

~~The~~ ~~enable~~

From the function table →

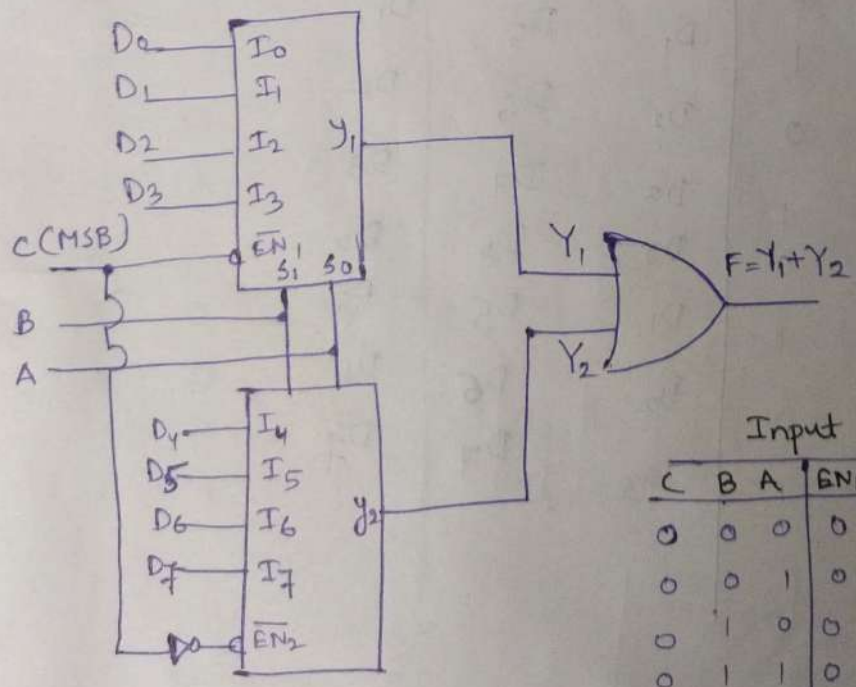
$$Y = (\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3)\,\overline{EN}$$



4:1 MUX using NAND gates.

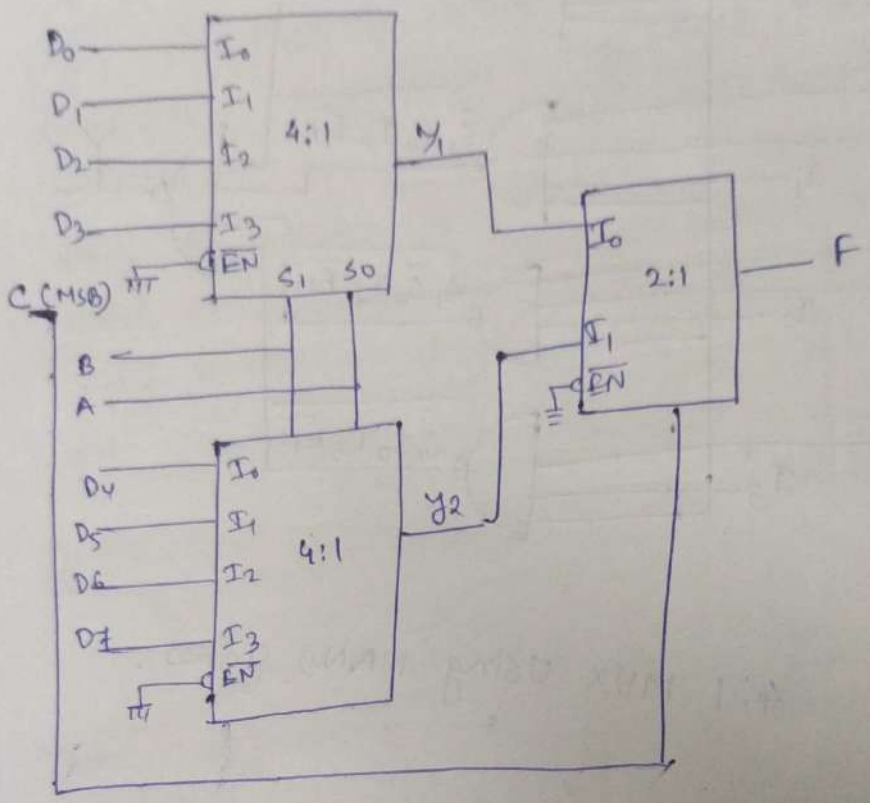
Cascading of Multiplexer :→

Design of 8:1 MUX using two 4:1 MUXs and OR gate :→



Input					Output		
C	B	A	EN_1	EN_2	Y_1	Y_2	F
0	0	0	0	1	D_0	0	D_0
0	0	1	0	1	D_1	0	D_1
0	1	0	0	1	D_2	0	D_2
0	1	1	0	1	D_3	0	D_3
1	0	0	1	0	0	D_4	D_4
1	0	1	1	0	0	D_5	D_5
1	1	0	1	0	0	D_6	D_6
1	1	1	1	0	0	D_7	D_7

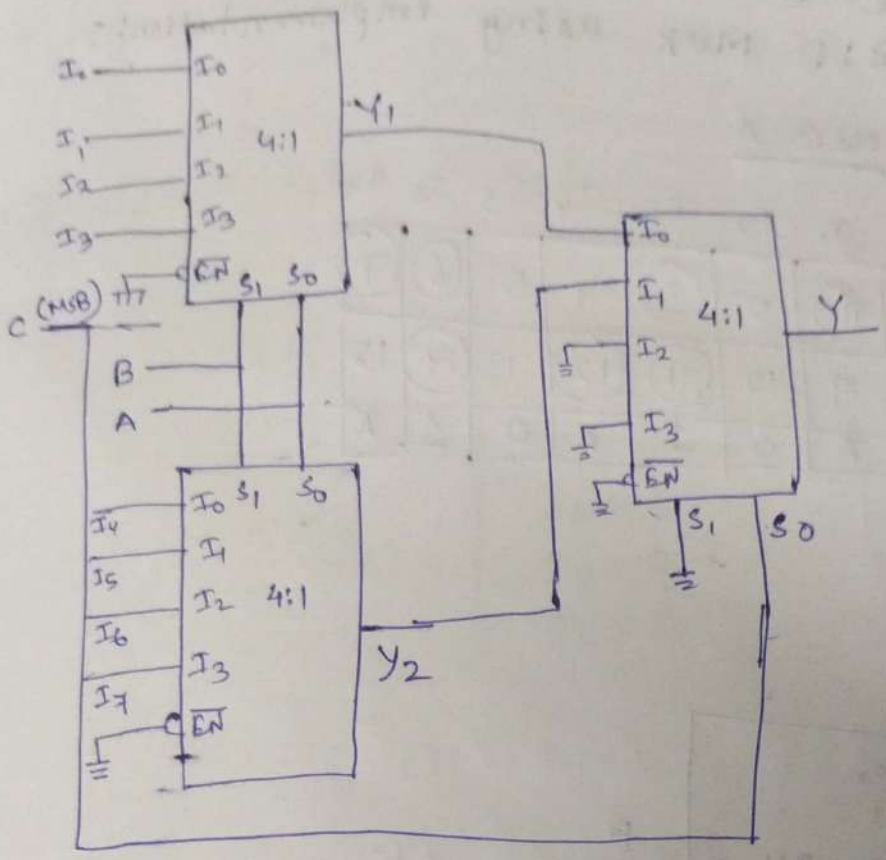
Design of 8:1 MUX using Two 4:1 MUX and 2:1 MUX:-



Function table:-

Input			output		
C	B	A	Y_1	Y_2	F
0	0	0	D_0	D_4	D_0
0	0	1	D_1	D_5	D_1
0	1	0	D_2	D_6	D_2
0	1	1	D_3	D_7	D_3
1	0	0	D_0	D_4	D_4
1	0	1	D_1	D_5	D_5
1	1	0	D_2	D_6	D_6
1	1	1	D_3	D_7	D_7

Desing and 8:1 MUX using only 4:1 MUX:-



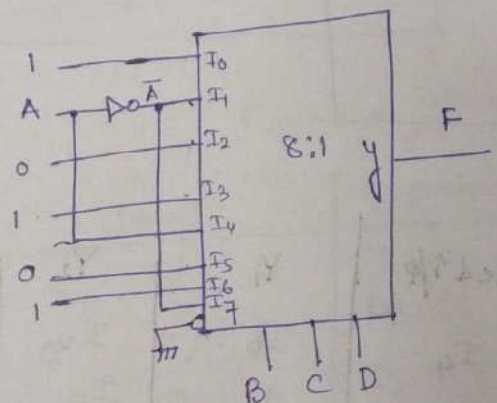
Selected lines			Selected i/p	Y_1	Y_2	output Y
C	B	A				
0	0	0	I_0, I_4	I_0	I_4	I_0
0	0	1	I_1, I_5	I_1	I_5	I_1
0	1	0	I_2, I_6	I_2	I_6	I_2
0	1	1	I_3, I_7	I_3	I_7	I_3
1	0	0	I_0, I_4	I_0	I_4	I_4
1	0	1	I_1, I_5	I_1	I_5	I_5
1	1	0	I_2, I_6	I_2	I_6	I_6
1	1	1	I_3, I_7	I_3	I_7	I_7

MUX As a Logic Function generator using Implementation table Method :-

Implement the function $F = \Sigma m(0,1,3,6,7,8,11,12)$ using a 8:1 MUX using implementation

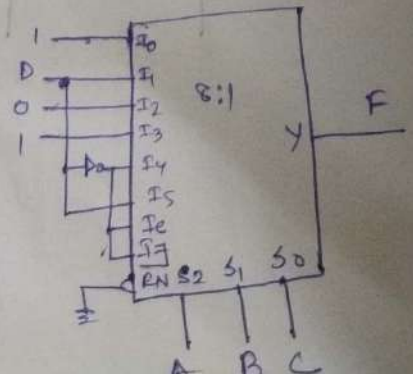
Soln using MSB A

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	1	$\bar{A}$	0	1	A	0	1	$\bar{A}$

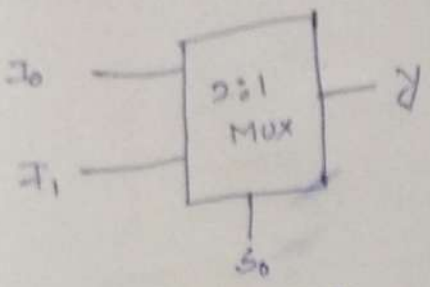


using LSB D

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{D}$	0	2	4	6	8	10	12	14
D	1	3	5	7	9	11	13	15
	1	D	0	1	$\bar{D}$	D	$\bar{D}$	$\bar{D}$



Multiplexer as Universal Logic Module :-



$Y = \bar{S_0} I_0 + S_0 I_1$

1) AND gate :-

$X = AB$

$Y = \bar{S_0} I_0 + S_0 I_1$

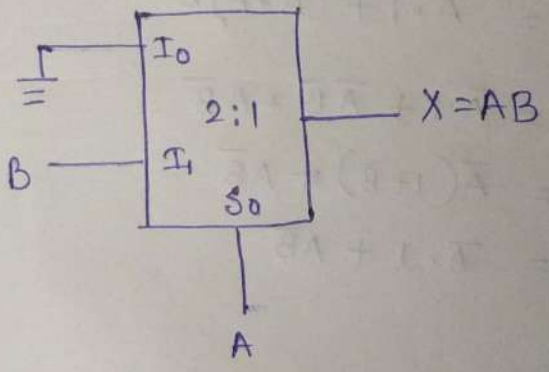
$X = \bar{A} \cdot 0 + AB$

by Compairing

$S_0 = A$

$I_0 = 0$

$I_1 = B$



2) OR gate :-

$Y = A + B$

$= A + B(A + \bar{A})$

$= A + AB + \bar{A}B$

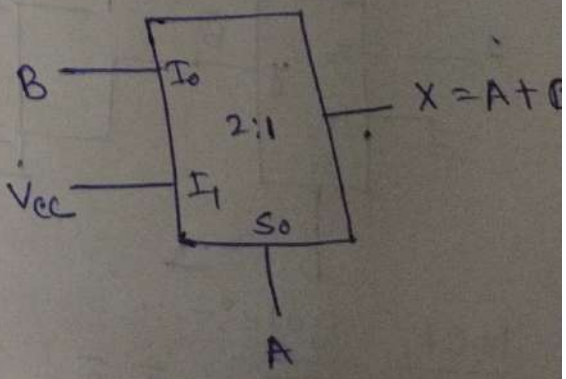
$= \bar{A}B + A(1 + B)$

$= \bar{A}B + A \cdot 1$

Therefore, $S_0 = A$

$I_0 = B$

$I_1 = 1$



3) NOT gate ⇒

$X \Rightarrow \overline{A}$

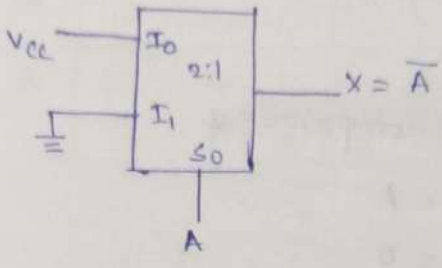
$Y \Rightarrow \overline{S_0} I_0 + S_0 I_1$

$\Rightarrow \overline{A} \cdot 1 + A \cdot 0$

So, $A = S_0$

$I_0 = 1$

$I_1 = 0$



4) NAND gate :-

$$F = \overline{AB} = \overline{A} + \overline{B} = \overline{A} \cdot 1 + (\overline{A} + A)\overline{B}$$

$$= \overline{A} \cdot 1 + \overline{A}\,\overline{B} + A\overline{B}$$

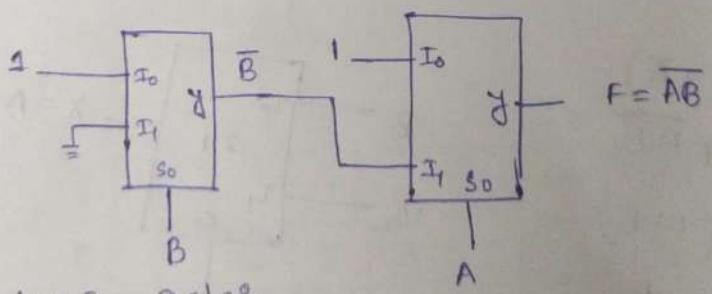
$$= \overline{A}(1 + \overline{B}) + A\overline{B}$$

$$= \overline{A} \cdot 1 + A\overline{B}$$

So, $S_0 = A$

$I_0 = 1$

$I_1 = \overline{B}$



5) NOR gate :-

$F = \overline{A+B} = \overline{A} \cdot \overline{B} = \overline{A} \cdot \overline{B} + A \cdot 0$

Therefore, $S_0 = A$, $I_0 = \overline{B}$, $I_1 = 0$