

**VIVEKANANDA COLLEGE  
THAKURPUKUR  
KOLKATA-700063**

**NAAC ACCREDITED 'A' GRADE**



Topic: Control Signal and Address Decoding

Course Title: Microprocessor and its Application

Paper: CMS-A-CC-4-10-TH

Unit: Microprocessor Architecture and Memory Interfacing

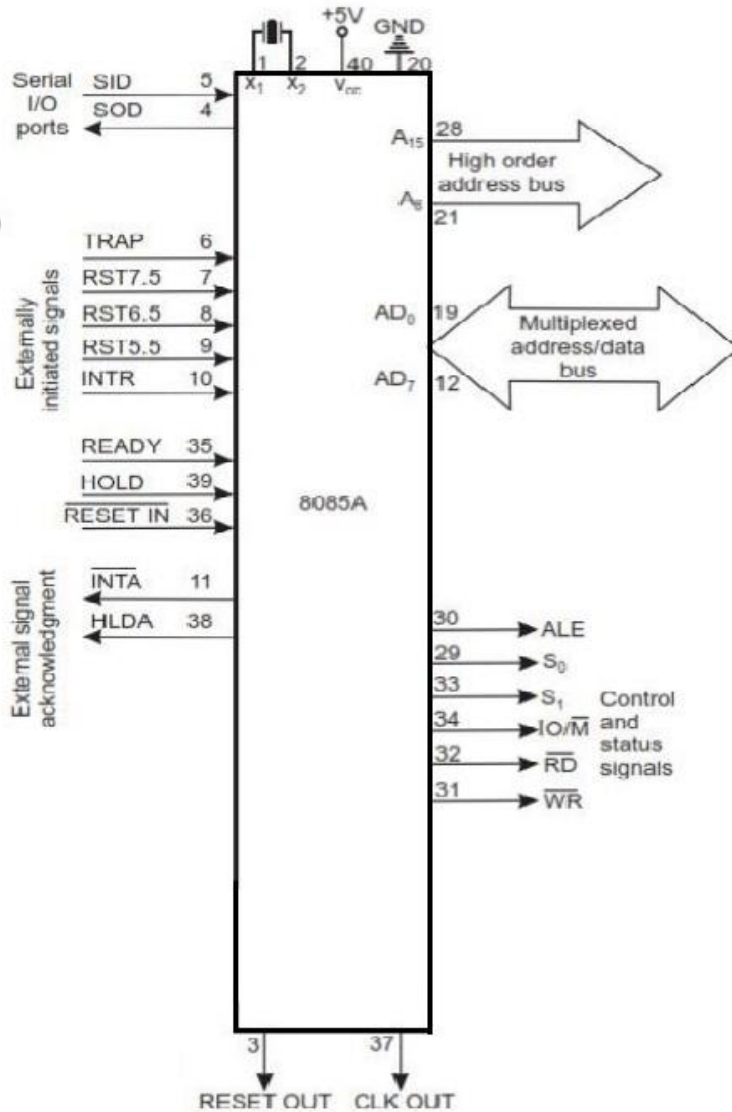
Semester: 4<sup>th</sup> Semester

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Control and Status signal:

8085 microprocessor has got three status signals  $S_0$ ,  $S_1$  and  $IO/\bar{M}$  and a special signal ALE.



$\overline{RD}$  – It is a read control signal. When the signal on this pin is low, selected memory on input output device is read and the information is placed on the data bus.

$\overline{WR}$ – It is a write control signal. When the signal is low, the data on the data bus is return to the memory or input output device

$IO/\bar{M}$ – When the signal on this pin is high, microprocessor performs input output related operations. When the signal on this pin is low, microprocessor performs memory related operations.

$\bar{R}D$	$\bar{W}R$	$IO/\bar{M}$	
0	1	1	Microprocessor reads data from I/O device.
0	1	0	Microprocessor reads data from memory.
1	0	1	Microprocessor writes data from I/O device.
1	0	0	Microprocessor writes data from memory.

### ALE – Address Latch Enable

It is used to latch low order 8 – bit address present on  $AD_0 – AD_7$  into external latches.

### Signals $S_0$ & $S_1$

It is used to indicate the current status of the processor.

$IO/\bar{M}$	$S_1$	$S_0$	States
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch

### Serial I/O Port:

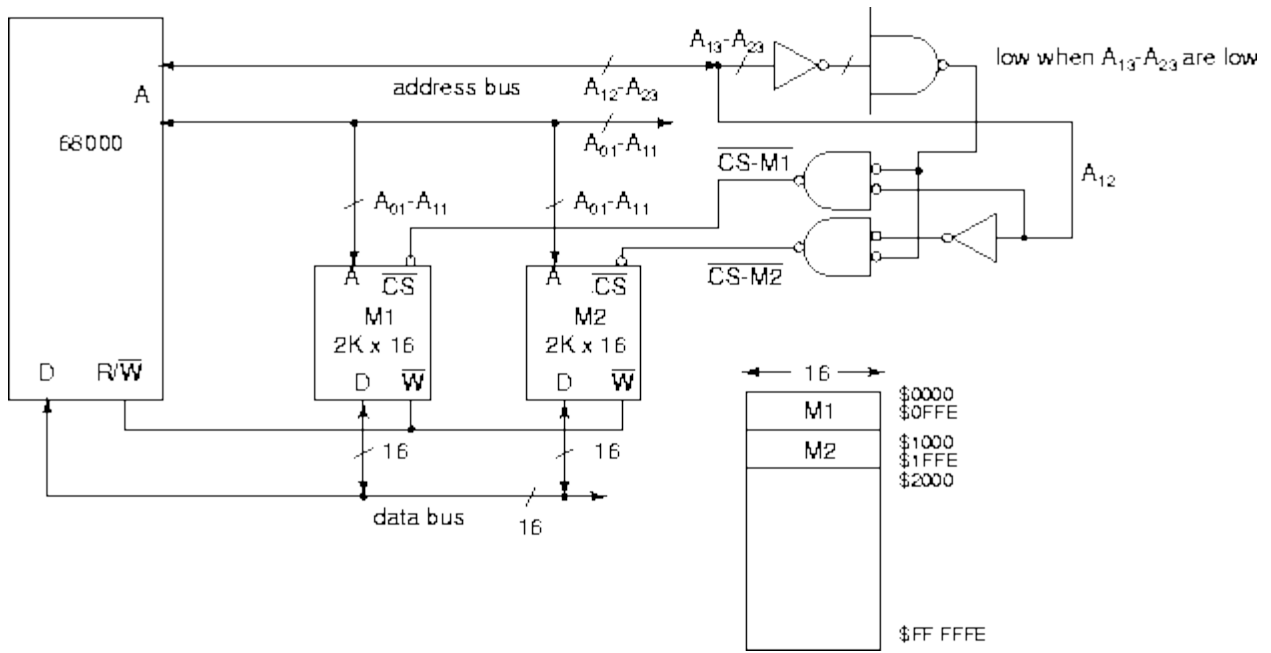
**SID and SOD** – Pair of signals used for serial I/O communications.

- **SID** ( Serial Input Data)-Serial data is read by the microprocessor via SID line.
- **SOD** (Serial Output Data)-Serial data is given out of the microprocessor via SOD line.

**Address decoding** refers to the way a computer system decodes the addresses on the address bus to select memory locations in one or more memory or peripheral devices. The 68000's 23-bit address bus permits  $2^{23}$  16-bit words to be uniquely addressed.

In **full address decoding**, each addressable memory location corresponds to a unique address value on the address bus. Figure 126 shows an example of two memory devices configured using full address decoding. Memory M1 is selected

whenever  $A_{12}-A_{23}=000000000000$ , while M2 is selected whenever  $A_{12}-A_{23}=100000000000$ .



In **partial address decoding**, not all address lines in the address bus are used in the decoding process. Figure 127 shows two memory devices configured using partial decoding, where  $A_{23}$  is used to distinguish between the two. In this example, M1 and M2 are repeated 2,048 times through the memory space. When  $A_{23}=0$ , M1 is selected; when  $A_{23}=1$ , M2 is selected.

