VIVEKANANDA COLLEGE
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NAAC ACCREDITED 'A' GRADE

Topic: Input output characteristics of Bipolar Junction Transistor.

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The characteristics of the transistor is generally refers the static characteristics. Since in this device the number of terminals are three and any two port network contains one port as input and other port as output, one terminal should be common to both input and output port. The mode of connection is also defined by the common terminal namely

i) Common base (CB) mode: base is common to both input and output circuit.

ii) Common emitter (CE) mode: emitter is common to both input and output circuit.

ii) Common collector (CC) mode: collector is common to both input and output circuit.

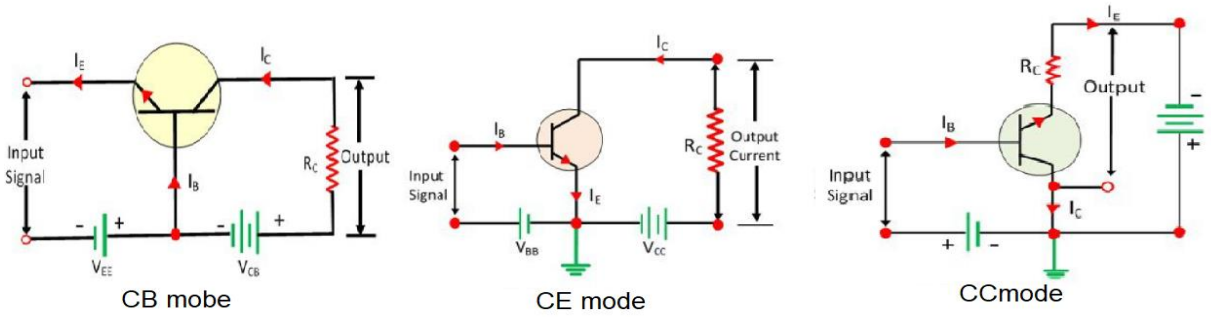
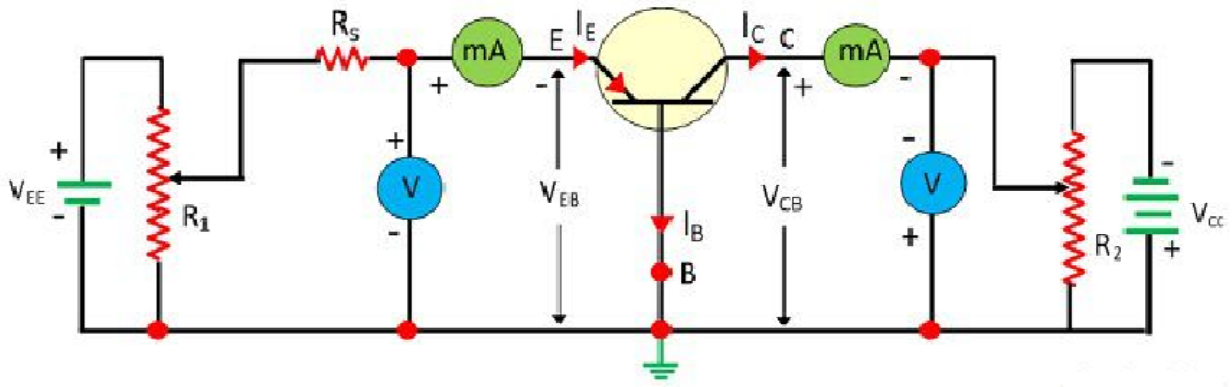


Figure 1 showing different mode of NPN transistor

The structures and characteristics of the emitter, base and collector are different. So characteristics differ from mode to mode. It was also observed that some mode is suitable for some specific applications. Here we study the characteristics of CB, CE and CC modes.

Characteristics of CB mode:

The circuit plan to study CB mode characteristics is described in the following figure.2



The circuit plan to study CB mode characteristics

Figure 2

Since base is the common terminal to input and output circuit. In the input section we have V_{EB} the emitter voltage with respect to the base as controlling voltage and that for output as V_{CB}, base to collector voltage. Input current is the emitter current I_E and output current is collector current I_C. We have the following characteristics:

1) **Input characteristics**: *Variation of emitter current for different base to emitter voltage keeping output voltage (base to collector voltage) constant*. The input characteristics curves are I_E versus V_{EB} curve while V_{CB} constant.
2) **Output characteristics**: Variation of collector current I_C for different base to collector voltage V_{CB} for constant input current (emitter current I_E). The output characteristics curves are I_C versus V_{CB} curve while I_E constant.
3) **Transfer characteristics or current gain characteristics**: variation of collector current I_C for different emitter current I_E keeping output voltage V_{CB} constant.

1. Input characteristics:

Input junction is simply a pn junction diode kept in forward bias. So a variation of V_{EB} will just produce a diode current which can be taken as the input current or emitter current I_E. For a pnp transistor. Emitter, the p end is connected to higher potential and the base, the n end is connected to lower potential. So V_{EB} should be positive. (***E end is positive with respect to the B end***). Under the forward bias current will flow through emitter to base i.e., p end to n end. The basic nature of the curve reminds the forward characteristics curve of diode. A certain voltage is required to get the conduction through the junction. This is the cut-in or offset or threshold voltage. The reason for existence of this voltage is same as was observed for pn junction. Its value varies near about 0.7 volt for silicon.

As I_E depends on V_{EB} and V_{CB} one can express emitter current as

$$\mathbf{I_E = I_E\ (V_{EB}, V_{CB})}$$

For different values of V_{EB} we have a series of curves for I_E , Or we can seek the variation in I_E for different values of V_{EB} for a specific value of V_{CB}.

Upto this point we did not mention V_{CB}. Let us consider V_{CB} as negative voltage, which means collector is at lower potential than the base. This arrangement obviously makes the J_{CB} in reverse bias. Because collector is of p type and it is connected to the negative end of the battery. It was observed that *when magnitude of V_{CB} increases i.e., collector becomes more and more negative with respect to the base emitter current increases for a specific V_{EB}*. The reason is that as V_{CB} becomes more negative depletion region width at J_{CB} increases. Depletion region penetrates

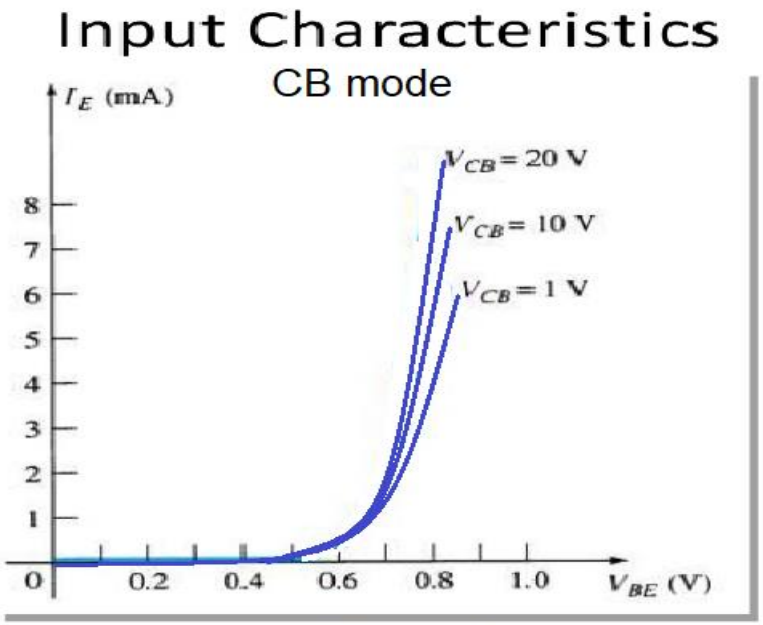


Figure 3

more inside the base region due to lower doping concentration of the base. Effective base region, *which helps to conduct*, decreases. This decreases the resistance of the emitter base pn junction. The increment discussed here is very small and will be observable for substantial change of the collector base voltage. The cut in voltage more or less same for all V_{CB} .

Figure 3: Input characteristics for CB connection

2. **Output characteristics**:

The output junction J_{CB} is at reverse bias by the voltage V_{CB}. The carriers injected from emitter after traversing the base appear at the collector. So collector current is always present which is comparable to the emitter current for a small voltage V_{CB}. Keeping emitter current constant if V_{CB} changes the enhancement in collector current is almost negligible. The increment of negative V_{CB} makes collector end more negative which helps to attract the majority carriers present in the collector. For a constant I_E there is no chance to increase the number of carriers not only that the minority carrier current I_{CBO} that also becomes constant after a small V_{CB}. Thus the characteristic curves are almost parallel to the voltage axis.

Though a little but a definite increment of collector current is observed for increment of V_{CB}. It is already discussed that for higher V_{CB} value effective base region decreases. The decrement of the base region reduces the recombination loss in

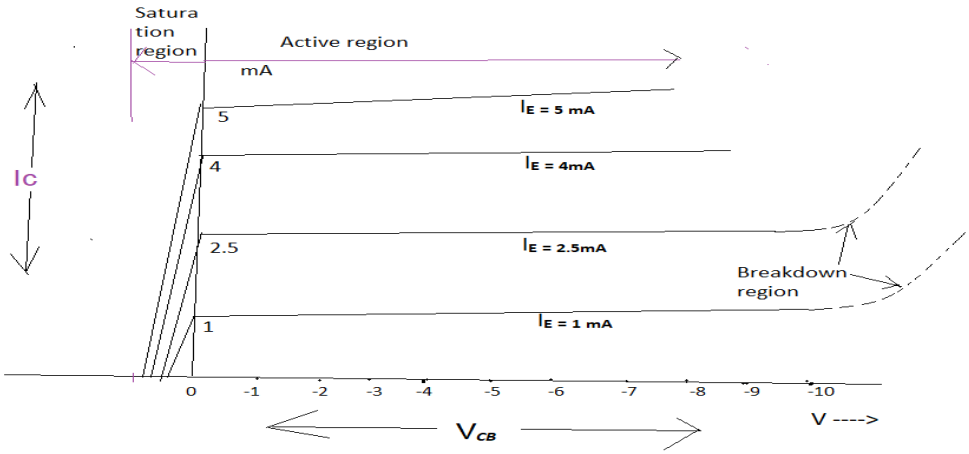


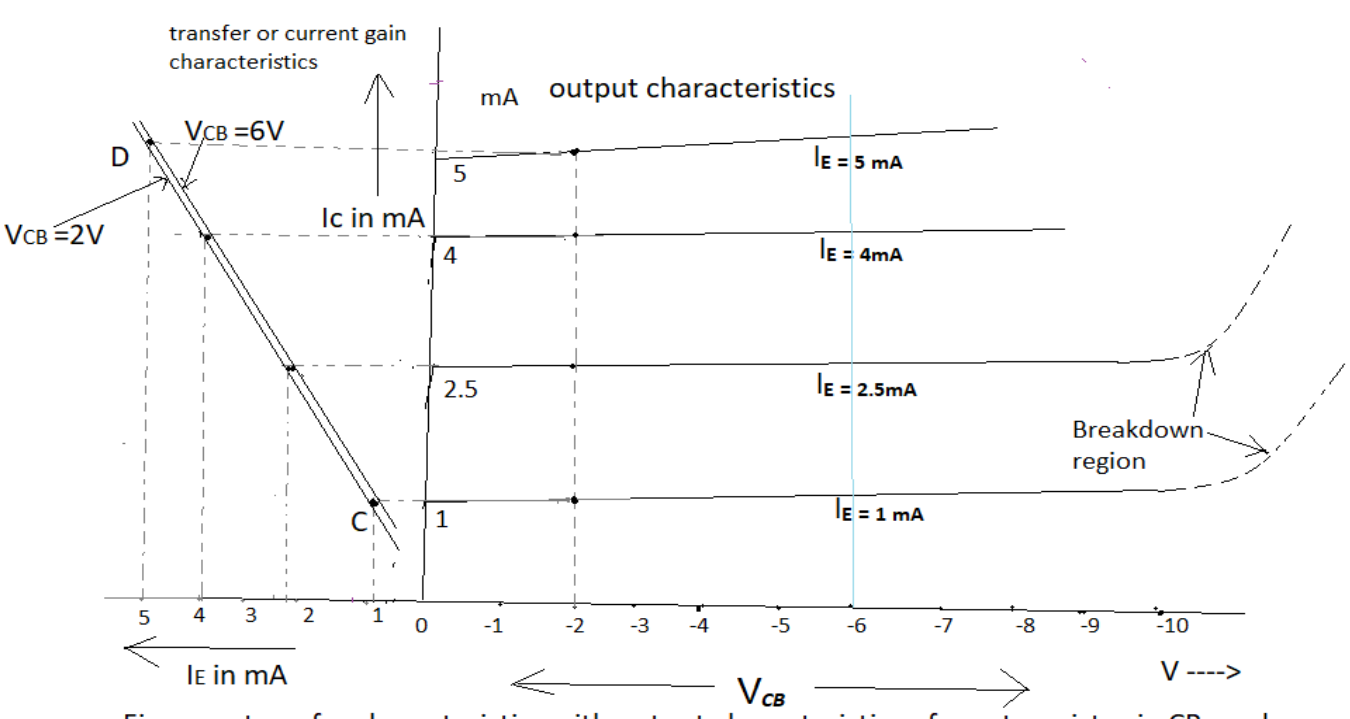
Figure 4: Output characteristics of pnp transistor in CB modes

the base. This causes a small increment of the collector current.

The reduction of base width by the application of the reverse voltage in the output circuit is known as ***early effect***. If we increase the V_{CB} more the depletion region occupies the whole base region and depletion region of the junction J_{CB} comes into the contact of the depletion region of the J_{EB} junction. This condition is known as *punch-through* or *reach through*. *If the V_{CB} increased more than the voltage for punch through there lies always a possibility to get reverse breakdown in the J_{CB}.*

Transfer characteristics:

This can be measured from the output characteristics also. For a constant V_{CB} base recombination is constant and collector current becomes proportional to the emitter current. For the increment of V_{CB} collector current will be enhanced due to the early effect. This enhance becomes much more prominent in this curves than the output characteristics curve.



The current gain in this mode is $\alpha = I_C/I_E$ ----------(1)

So the collector current can be written as $I_C = \alpha I_E$. Considering the minority carrier current which is also flowing outward we have

$I_C = \alpha I_E + I_{CBO}$ ----------(2)

Or $\alpha = (I_C - I_{CBO})/I_E$ ----------(3)

Depending upon the value of the collector current and the condition of the junction J_{CB} the output characteristics curves can be divided into three regions: active, cut off and saturation region.

Active region: In this region J_{CB} is biased in the reverse direction and the J_{EB} is biased in the forward direction. In this region characteristics curves maintain a regular separation and the current gain also more or less constant. Disregarding the change of I_C due to early effect the collector current is essentially independent of collector voltage V_{CB} and solely depends on the emitter current. So for regular variation of the input current or emitter current output current also varies regularly. This region is used for most of the application of transistor. To get a faithful amplification (without distortion of wave form) transistor should be operated in the active region.

Cut off region: In this region emitter current is zero. Since emitter current is the main source of carrier, without it we can consider almost no current in the region and hence the nomenclature. However, the current is not really zero. We know that $I_C = \alpha I_E + I_{CBO}$. Therefore $I_C = I_{CBO}$ in absence of the emitter current. We have the idea about the magnitude of that current. This is nothing but reverse saturation current in the reverse biased collector base pn junction. For the silicon devices it varies from n A to μA. Whereas the magnitude of the collector current is of the order of mA. I_{CBO} is the minimum value of the current in the collector circuit. So the region for which $I_C < I_{CBO}$ is known as cut off region. Transistor is considered as off or non-conducting in this region.

Saturation region: The nomenclature is somewhat misnomer. Since we are talking about the variation of collector current the name creates a sensation as if the current becomes saturated. It was found that people sometimes consider a typical characteristics curve for a specific input current and realise the active region as saturation region because output current becomes constant at that level! *It is worthwhile to mention that the current is not determined by the characteristics curve only but with the load line also (the clear view of Load-line will be given in CE mode)*. (This region resides on the side where the load line meets the current axis. The meeting point is the maximum current in that circuit (voltage divided by the net load resistance in the circuit). Voltage and current vary along the load line. The intersection point of the transistor characteristics curve with the load line gives the output voltage and current. Any characteristic curve can be chosen by proper choice of the input current I_E and hence the output current be fixed. If the operating voltage is very near to saturation region then current will be maximum on this device. From this point of view device is saturated with the Currents

The requirement for saturation region is that both the junctions J_{EB} and J_{CB} are forward biased. The forward biased J_{EB} emits the carriers but forward bias J_{CB} is not ready to accept them. Forward biased J_{CB} indicates the p type collector is connected to positive end of the battery. The positive terminal tries to repel the holes. So the collector currents falls down very quickly and becomes zero within a few volts. This referred as bottoming of the collector current. In CB mode operation it is in the positive side of the V_{CB} axis (for pnp transistor).

Transistor switching action always rely on the two states cut off and saturation for off and on condition of the switch.

Study of this region is very difficult in this sense of the voltage be increased more than the value required to stop the collector current collector base junction behaves like emitter and injects carrier through the base into the emitter. Under this condition one can define a different parameter α_R, reverse current gain.

Characteristics of CE mode

The circuit plan to study CE mode characteristics is described in the following diagram.

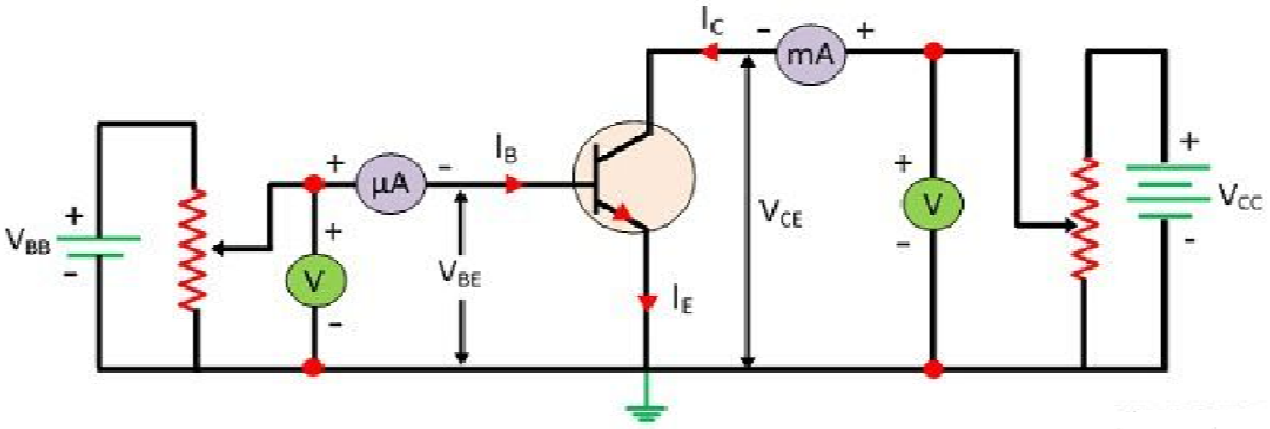


Figure 6: circuit diagram to study CE mode characteristics for npn transistor

Here emitter is common to the input and output circuit. Base and emitter make the input port whereas output port is made of collector and emitter. Under this arrangement base current I_B is the input current and collector current I_C is the output current. V_{BE} is the controlling voltage in the input port. Output is controlled by $\mathbf{V_{CB}}$. Like the CB mode we should study the following characteristics:

Input characteristics: variation of input current I_C for variation of V_{BE} under the constant V_{CE}.

Output characteristics: variation of output current I_C for variation of V_{CE} under the constant input current I_B.

Transfer characteristics: variation of collector current I_C with variation of input current or base current I_B for constant V_{CE}.

Before discussing the characteristics curves let us concentrate on basic mode of connection of the transistor in this mode. Here output circuit includes two extreme ends of the device the emitter and collector. When we discuss the current components we make a comment that carriers start their journey from emitter and ended at collector. This is true here also. But unlike the CB connection where emitter was really in input circuit and collector in output circuit here both the terminals are the members of the output circuit. Though emitter is a member of the input circuit the same is the member of the output circuit. So it is impossible to excite emitter separately without affecting the output circuit. That creates the complexity.

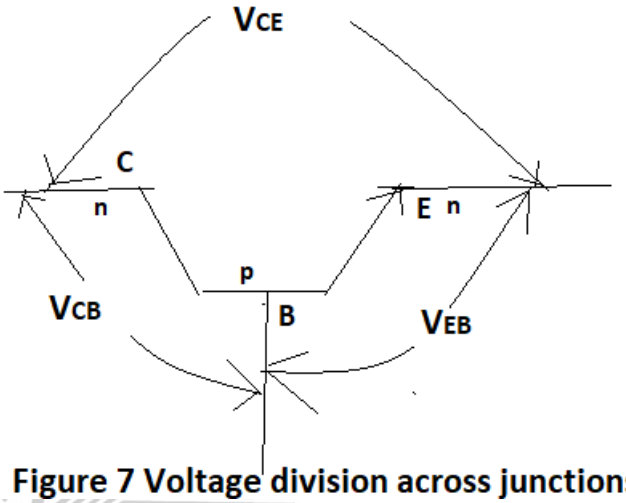


Figure 7 Voltage division across junctions

Let us have a look at the following figure. From the figure it is obvious that

$V_{CE} = V_{CB} + V_{BE}$ ---------(4)

For npn transistor collector is of n type. So to collect majority carriers, electrons from collector it should be connected with the +ve end of the supply that indicates V_{CE} should be +ve. In other words collector becomes more +ve than the emitter. As we go towards the collector end from the emitter end upper portion remains in higher potential than the lower portion. This situation is depicted in the adjacent diagram with resistors. Since the upper end is +ve of the assembly then for any resistance upper end is +ve means at higher potential than the bottom of that resistance which is denoted by a -ve sign.

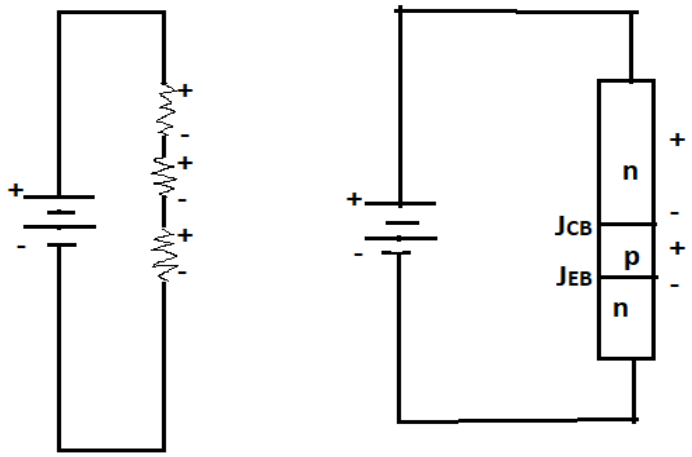


Figure 8 potential gradient along the transistor

Look at the transistor diagram. The same type of potential gradient will be created throughout the semiconductor bar. Just like the resistance assembly we can put +ve and -ve sign do denote higher and lower potential ends. If we want to make the collector +ve that makes J_{CB} in reverse bias no doubt but the same arrangement make J_{BE} in forward bias. Some one can say "ok, we have achieved our goal. With a single supply we make emitter in forward bias and collector in reverse bias!" We have no objection about this achievement but want to mention one thing is that this forward biasing is in not our control. If we connect collector and emitter with a piece of wire that indicates $V_{CE} = 0$. Under such condition if we make V_{BE} +ve (base at higher potential than emitter) V_{CB} becomes -ve (collector at lower potential than base) to make V_{CE} zero. That simply means collector becomes biased in forward direction.

Input characteristics A careful look always reveals that again we have a pn junction in the input section. So one can expect the characteristics like forward characteristics of pn junction because J_{BE} should be in forward bias condition to activate emitter. There is a difference with ordinary pn junction is that base width (p region of npn transistor) is very small and doping concentration is much much lower than emitter. A very small fraction of the emitter current can be found in the base or input terminal. Due to this reason the nature of the curve becomes similar to the diode curve but the magnitude of the current becomes very small of the order of µA.

The dependence of input current can be written as $I_B = I_B (V_{BE}, V_{CE})$. So a family of curves can be obtained by varying V_{CE}, voltage at the output terminal. An increment in V_{CE} increase the reverse bias of the junction J_{BC} . Effective base region decreases which decreases recombination in base and current flowing through this terminal. Though there is an enhancement of the junction J_{BE} this can not counterbalance the previous effect. So the main two differences with the input characteristics of common base are a) magnitude of current is very small, b) current decreases for increment of the output voltage.

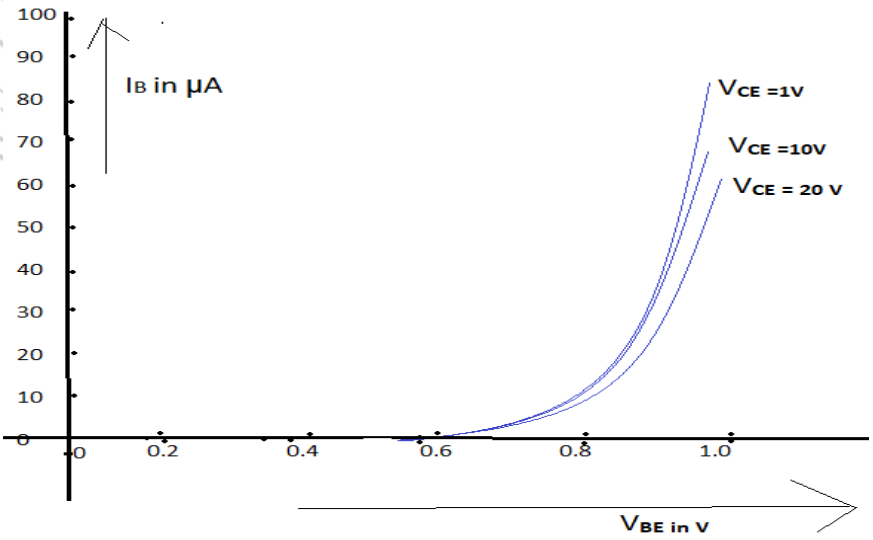


Figure 9 input characteristics of CE mode

Output characteristics Output characteristics of CE mode is the variation of collector current for the variation of emitter to collector voltage V_{CE}. Here input current, I_B is considered as parameter. Analytically it can be written as $I_C = I_C (V_{CE}, I_B)$. The family of curves are obtained for different value of the base current. The carrier emitted by the emitter is collected at collector. Let us consider from a considerable value of voltage V_{CE}. In presence of V_{BE} emitter is already in forward bias. In this condition the increment of V_{CE} increase the collector current in two ways

a) It reduces the effective base width by *early effect* which reduces recombination in the base and enhances the collector current.

b) Enhances the V_{BE}.

Under the two effects the current increase slowly with increment of V_{CE}. Most of the effect goes to the base reduction process. A small change in base current is reflected in the collector current with a large fraction because there is a difference of the factor 10^3 (base current ~ µA and collector current mA). The curves possesses more slope than the slope of the curves of CB mode. If we extrapolate the curves, all of them will meet at a definite point on the positive value of the output voltage axis. This voltage is referred as *early voltage*. The magnitude of the early voltage varies between 60 to 100 volts, whereas the transistor characteristics curves are described within 12 volts. This reference of the two voltages is enough to realise how small the slopes are.

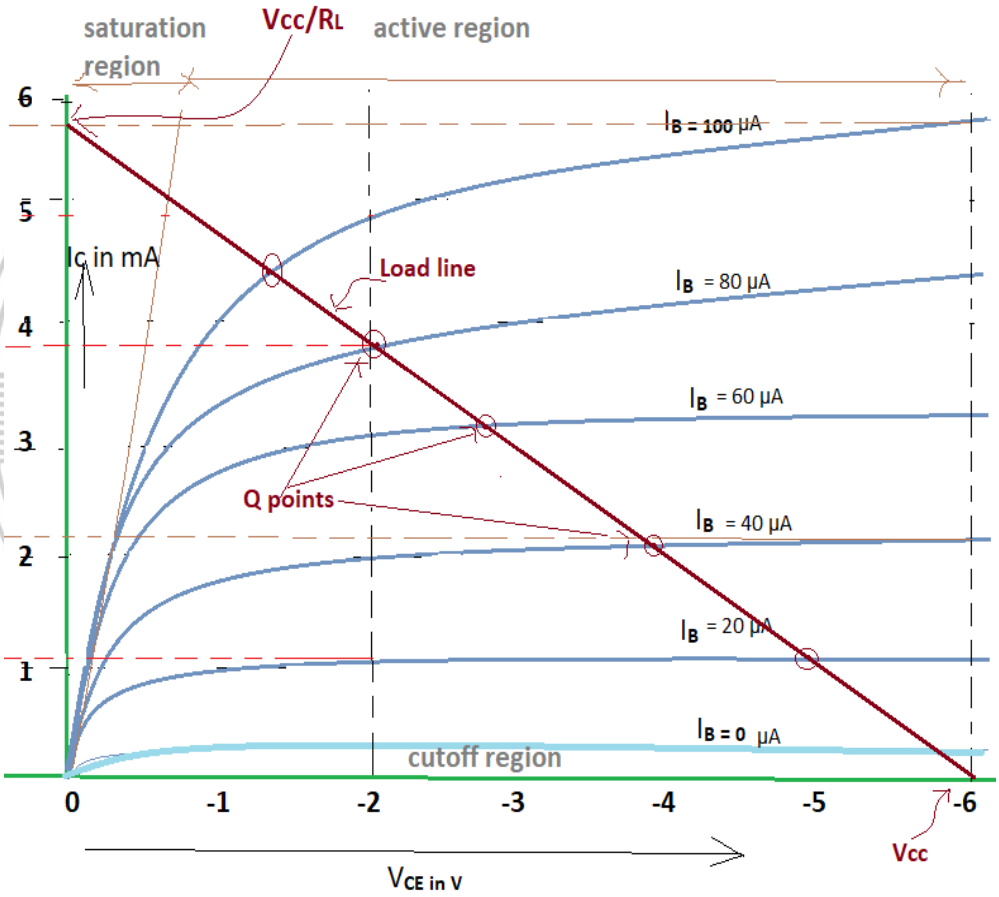
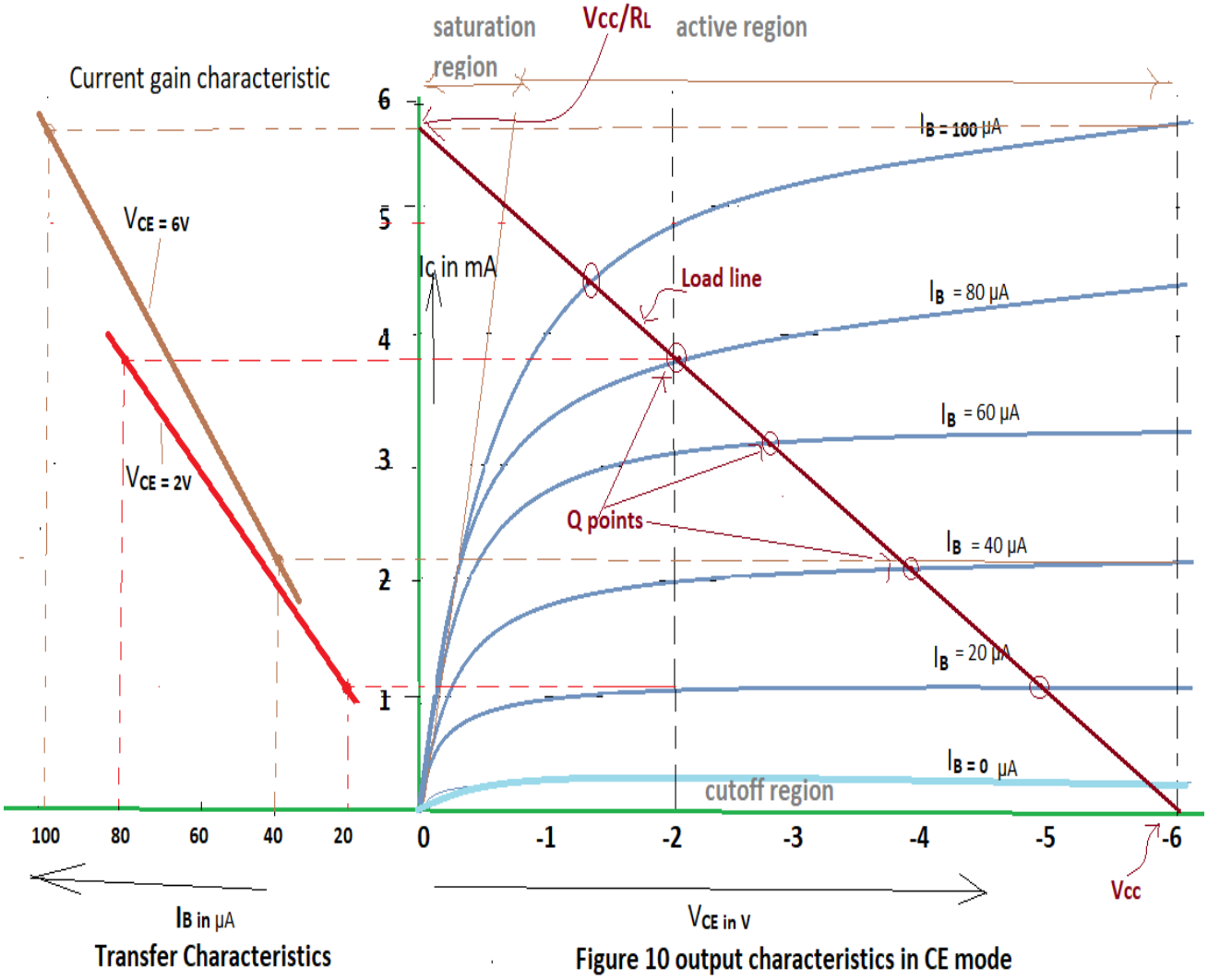


Figure 10 output characteristics in CE mode

Transfer characteristics: This is the variation of collector current I_C for variation of the base current I_B when output voltage V_{CE} is kept constant. Here current gain is defined as

$\beta = I_C / I_B$



Transfer Characteristics

Figure 10 output characteristics in CE mode

In any higher value of V_{CE} collector current should increase for a fixed base current. But the most interesting thing is that (which was not observed for CB output curves) current gain i.e., the slope of the curves also changes. So β is function of the collector emitter voltage V_{CE}.

We have observed α and β are interrelated. Infect, the value of a changes but the change of collector current is very small for base width modulation which becomes much more prominent in CE mode when base current is related with the input circuit.

$$\boldsymbol{\alpha = \frac{IC}{IE}}$$

And

$$\boldsymbol{\beta = \frac{IC}{IB}}$$

$$\boldsymbol{\beta = \frac{\gamma B}{1 - \gamma B} = \frac{\alpha}{1 - \alpha}}$$

The last one shows the interrelationship between **α** and **β**. So that if **α** is known to anybody **β** can be calculated easily. It can be shown that

$$\boldsymbol{\alpha = \frac{\beta}{1 + \beta}}$$

Now we have from equation (2)

$I_C = \alpha I_E + I_{CBO}$

$= \alpha(I_B + I_C) + I_{CBO}$

$I_C - \alpha I_C = \alpha I_B + I_{CBO}$

$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

$I_C = \beta I_B + (1 + \beta) I_{CBO}$

$I_C = \beta I_B + I_{CEO}$ ----------(5)

This equation is similar to the equation (2) observed for CB mode. The first term βI_B gives the collector current due to certain amount of input current I_B, but the second term may arise without the presence of I_B. So this is open circuit current in CE mode. So the name is suggested as I_{CEO}. The magnitude of this current can be assuned from the following relation.

$I_{CEO} = (1 + \beta) I_{CBO} \approx \beta I_{CBO}$ ----------(6)

I_{CBO} was found as simply the reverse saturation current of a reversed biased diode (J_{CB} pn junction). Here it is β times larger than that. I_{CBO} ~ uA and standard value of β ~ 100, so the I_{CEO} becomes some fraction of mA. This value cannot be neglected and becomes an important factor for conduction process.

The CE mode is mostly used mode because its high current gain. The large amount of open circuit current compelled us to take extra protection and demands proper design. Before going to discuss the different output region let us try to realise physically the origin of such large open circuit current.

When collector is kept at reverse biased condition to collect, the carriers with input i.e., base-emitter open, J_{CB} becomes reversed biased and J_{EB} forward biased. The reverse biased J_{CB} generates a reverse saturation current I_{CBO}. This I_{CBO} consists of flow of holes from base to collector and electrons from collector to base. The forward biased J_{EB} injects electrons in the base regions. Since input (base) is open there is no chance of recombination. These newly injected electrons increases the minority carrier density inside the base. Eventually this is nothing but I_{CBO}. When these holes enter inside the collector they should follow the amplification β. Therefore the part of the collector current for these injected carriers from the J_{EB} becomes $\beta\ I_{CBO}$. The total open circuit current thus comes out to be $(I_{CBO} + \beta\ I_{CBO}) = (1 + \beta)\ I_{CBO}$.

Like the output curves of the CB mode we can also divide the output characteristics into three several regions: cut off, active and saturation regions.

Cut off region: The minimum current in CE configuration is the open circuited current flowing through the device I_{CEO}. Therefore the characteristics region for which collector current $I_C < I_{CBO}$ is considered as non-conducting region or cut off region.

Saturation region: Unlike the CB characteristics polarity of V_{CE} need not to be reversed to get saturation region. When V_{CE} is zero under the application of some voltage in the base emitter circuit J_{CB} becomes in forward bias. So condition for saturation becomes fulfilled at $V_{CE} = 0$. Infect within 1 volt of V_{CE} the saturation region ends. Here this region really lies at corner of maximum current of load line. The current gain here does not obey the linear law. In this region a new parameter β_{froced} is defined which changes with change of V_{CE} very rapidly.

Active region: In this region input and output current obeys a fair relationship which were discussed earlier. For transistor amplifier the no signal point is chosen in this region. Here the curves are more or less equispaced. So that variation of either side along load line (shown in fig 10) around a fixed point becomes more or less same. A faithful amplification becomes possible in this zone.